PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H02M 7/521, 7/525, H02J 9/06, H02H 7/122 — A1

(11) International Publication Number: **WO 98/59413**

(43) International Publication Date: 30 December 1998 (30.12.98)

(21) International Application Number: PCT/CA98/00602

(22) International Filing Date: 19 June 1998 (19.06.98)

(30) Priority Data:
2,208,380 20 June 1997 (20.06.97) CA

(71) Applicant *(for all designated States except US)*: AMSDELL INC. [CA/CA]; Unit 5, 45 Mural Street, Richmond Hill, Ontario L4B 1J4 (CA).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: WU, Fu, Ning [CN/CN]; Apartement 216, Building No. 313, Xhong Guan Cun, Haidan, Beijing 10080 (CN).

(74) Agent: BERESKIN & PARR; 40th floor, 40 King Street West, Toronto, Ontario M5H 3Y2 (CA).

(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: INTEGRATED UNINTERRUPTIBLE POWER SUPPLY PROTECTION SYSTEM WITH NOVEL INVERTER CIRCUIT

(57) Abstract

An uninterruptible power supply (UPS) system comprising an inverter for converting a DC voltage into an AC voltage comprising a full–bridge circuit having four silicon controlled rectifier (SCR) switches, two pulse control circuits for generating control voltage signals to turn on alternate pairs of said switches, a time sequencing circuit, and a power switch circuit. The full bridge circuit is directly connected to a positive DC input terminal and is coupled through the power switch circuit to a negative DC input terminal. The time sequencing circuit generates a first pulse signal for controlling the first pulse control circuit and a second pulse signal for controlling the second pulse control circuit so that the first pulse signal and the second pulse signal being in phase opposition. The time sequencing circuit further generates a third pulse signal for controlling the power switch circuit. The UPS inverter does not require an iron core transformer and so is of a size and weight which are compatible for use in small type UPS systems. Without sacrificing device size or safe and reliable operation, such a UPS system can be conveniently integrated physically with any standard power supply.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	**ES**	Spain	**LS**	Lesotho	**SI**	Slovenia
AM	Armenia	**FI**	Finland	**LT**	Lithuania	**SK**	Slovakia
AT	Austria	**FR**	France	**LU**	Luxembourg	**SN**	Senegal
AU	Australia	**GA**	Gabon	**LV**	Latvia	**SZ**	Swaziland
AZ	Azerbaijan	**GB**	United Kingdom	**MC**	Monaco	**TD**	Chad
BA	Bosnia and Herzegovina	**GE**	Georgia	**MD**	Republic of Moldova	**TG**	Togo
BB	Barbados	**GH**	Ghana	**MG**	Madagascar	**TJ**	Tajikistan
BE	Belgium	**GN**	Guinea	**MK**	The former Yugoslav Republic of Macedonia	**TM**	Turkmenistan
BF	Burkina Faso	**GR**	Greece			**TR**	Turkey
BG	Bulgaria	**HU**	Hungary	**ML**	Mali	**TT**	Trinidad and Tobago
BJ	Benin	**IE**	Ireland	**MN**	Mongolia	**UA**	Ukraine
BR	Brazil	**IL**	Israel	**MR**	Mauritania	**UG**	Uganda
BY	Belarus	**IS**	Iceland	**MW**	Malawi	**US**	United States of America
CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
CG	Congo	**KE**	Kenya	**NL**	Netherlands	**YU**	Yugoslavia
CH	Switzerland	**KG**	Kyrgyzstan	**NO**	Norway	**ZW**	Zimbabwe
CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
CM	Cameroon			**PL**	Poland		
CN	China	**KR**	Republic of Korea	**PT**	Portugal		
CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
EE	Estonia	**LR**	Liberia	**SG**	Singapore		

Title: Integrated Uninterruptible Power Supply Protection System with Novel Inverter Circuit

FIELD OF THE INVENTION

The present invention relates to an integrated UPS and power supply system, in which the UPS comprises an inverter circuit for converting a DC voltage into an AC voltage.

BACKGROUND OF THE INVENTION

Uninterruptible power supply (UPS) systems are commonly used for computers, fax machines, and other electronic devices. These systems provide protection against primary AC power failure and also against variations in power line frequency and voltage. There are generally three types of UPS systems: off-line or standby; line interactive; and on-line.

Off-line UPS systems do not regulate output voltage when the load is operating on utility power. As a result, off-line UPS systems are ineffective during power surges, spikes and brownouts, i.e. periods when a voltage reduction is initiated by a utility to counter excessive demand on its electric power generation and distribution system. In addition, when AC utility power is lost, an off-line UPS system requires a short transfer time before switching to battery power. These transfer times are typically several milliseconds, which makes off-line UPS devices unsuitable for use with sensitive equipment.

Line interactive UPS systems regulate voltage by adjusting the utility voltage before it passes to the load, and thus provide protection during brownouts and against power surges and spikes. However, these systems still exhibit transfer times of the order of a millisecond, and therefore are also unsuitable for use with sensitive equipment.

On-line UPS systems are connected between the power line and the load to provide for continuous voltage regulation and suppression of transients and noise. The transfer times for such systems are extremely small, and so they are suitable for very sensitive or highly critical

equipment. In addition, on-line UPS systems provide for an improved and more efficient utilization of input utility power, and the improved power factor helps lower energy costs.

UPS systems, especially on-line systems, are particularly valuable with respect to computer systems since they provide users with data and equipment protection. A significant number of computer system breakdowns are caused by utility power failures and fluctuations, and this may require that expensive hardware be replaced and software reinstalled. Power problems also often lead to lockups, crashes, lost data, and faulty data transmissions. For instance, users need power protection to ensure that an electronic data transfer via the internet is properly completed, without any loss of data or sensitive information, even in the event of a power failure. A significant amount of time may be expended and business lost in attempting to recover from power disruptions. Computers also now perform multiple functions such as sending faxes and answering telephone calls, making the need for power protection even greater.

Also, although power grids used by businesses may be more reliable than power grids for residential purposes, more and more people have begun working out of their homes. In addition, utility power supply in developing nations can be very inconsistent, with disruptions often occurring several times a day.

Typically, a UPS system includes a storage battery, a battery charger, a switching circuit, and an inverter circuit which converts a DC voltage into an AC voltage. Conventional inverter circuits typically employ push-pull circuitry to alternately drive the two primary windings of a transformer and generate an alternating positive/negative or AC signal at the secondary windings of the transformer. This type of inverter is widely used in small and medium UPS systems (i.e. below 1 kVA (kilo-voltamperes)), as well as in other equipment which converts DC voltage to AC voltage. Although such inverters are simple and reliable, they typically require low frequency (10-100 Hz) iron core transformers which are large, heavy, and expensive.

As a result, UPS systems which incorporate these inverters are large, bulky, and generally unsuitable for use with personal computers, fax machines, and other equipment requiring small UPS systems. Thus, while computer network server computer systems are often protected by UPS technology, this is much more rarely the case for individually based computers, despite the significant benefits provided by UPS systems. Current UPS technology is also expensive, particularly for on-line UPS systems.

There is therefore a need for a novel inverter circuit which operates in a reliable and stable manner but does not require an iron core transformer, and which can consequently be incorporated into a UPS device which is significantly smaller in size, lighter in weight, and more cost efficient than conventional UPS devices. Such a UPS system would provide further practical benefits if it could be integrated with a conventional power supply for specific types of electronic equipment, such as a personal computer.

SUMMARY OF THE INVENTION

In one aspect, the present invention comprises an inverter circuit (10) for converting a DC voltage between a first DC input (14) and a second DC input (16) into an AC voltage having first and second half cycles of opposite polarity across a load (6), said load (6) being coupled between a first output terminal (O1) and a second output terminal (O2), said inverter circuit (10) comprising

(a) a bridge circuit (3) comprising a plurality of silicon controlled rectifier switches (S1, S2, S3, S4) arranged in a bridge configuration, said bridge circuit being coupled between said first DC input (14) and a first node (15), said bridge circuit further being coupled to said first output terminal (O1) and said second output terminal (O2);

(b) a first pulse control circuit (1) responsive to a first pulse signal (I1) and coupled to said bridge circuit (3) for turning on a first portion (S1, S3) of said bridge circuit (3);

(c) a second pulse control circuit (2) responsive to a second pulse signal (I2) and coupled to said bridge circuit (3) for turning on a second portion (S2, S4) of said bridge circuit (3); and

(d) a timing circuit (4) coupled to said first and second pulse control circuits (1, 2) for generating the first pulse signal (I1) for controlling said first pulse control circuit (1) and the second pulse signal (I2) for controlling said second pulse control circuit (2), the first pulse signal and the second pulse signal being in phase opposition,

characterized in that:

(e) the inverter circuit (1) further comprises a power switch circuit (5) responsive to a third pulse signal (I3) and coupled between said first node (15) and said second DC input (16); and

(f) the timing circuit (4) is further coupled to the power switch circuit (5) and generates the third pulse signal (I3) for controlling the power switch circuit (5).

In another aspect, the present invention comprises an inverter circuit (10) for generating an AC voltage having first and second half cycles of opposite polarity and a wave form of a certain shape, said inverter circuit (10) converting a DC voltage between a first DC input (14) and a second DC input (16) into said AC voltage across a load (6), said load (6) being coupled between a first output terminal (O1) and a second output terminal (O2), characterized in that the inverter circuit (10) comprises:

(a) a bridge circuit (3) comprising a plurality of silicon controlled rectifier switches (S1, S2, S3, S4) arranged in a bridge configuration, said bridge circuit (3) being coupled between said first DC input (14) and a first node (15), said bridge circuit

(3) further being coupled to said first output terminal (O1) and said second output terminal (O2);

(b) a power switch circuit (5) responsive to a third pulse signal (I3) and coupled between said first node (15) and said second DC input (16);

(c) a first pulse control circuit (1) responsive to a first pulse signal (I1) and coupled to said bridge circuit (3) for turning on a first portion (S1, S3) of said bridge circuit (3);

(d) a second pulse control circuit (2) responsive to a second pulse signal (I2) and coupled to said bridge circuit (3) for turning on a second portion (S2, S4) of said bridge circuit (3);

(e) a timing circuit (4) coupled to said first and second pulse control circuits (1, 2) and to said power switch circuit (5) for generating a first pulse signal (I1) for controlling the first pulse control circuit (1), a second pulse signal (I2) for controlling the second pulse control circuit (2), the first pulse signal(I1) and the second pulse signal (I2) being in phase opposition, and a third pulse signal (I3) for controlling the power switch circuit (5);

(f) a circuit for providing a standard signal in the shape of said wave form;

(g) said inverter circuit being configured such that said first pulse signal (I1) pulses high and said second pulse signal (I2) remains low during the first half cycle of said standard signal; said second pulse signal (I2) pulses high and said first pulse signal (I1) remains low during the second half cycle of the standard signal; said third pulse signal (I3) pulses high if the value of said AC voltage is less than the value of said standard signal; and said third pulse signal (I3) remains low if the value of said AC voltage is greater than the value of said standard signal.

In a further aspect, the present invention comprises an integrated uninterruptible power supply (UPS) and power supply system (50) for protecting a device from disruptions in utility AC power, said device having a power supply circuit (62) installed thereon for receiving utility AC power installed thereon, characterized in that said integrated UPS and power supply system comprises said power supply circuit (62) and an uninterruptible power supply system circuit (52), said uninterruptible power supply system circuit comprising a battery (58) and an inverter circuit (10), said inverter circuit not having an iron core transformer and being of small size. The integrated UPS and power supply system preferably comprises an inverter circuit in accordance with the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings which illustrate preferred embodiments of the invention:

Fig. 1 shows an inverter circuit which can be incorporated in a UPS system in accordance with one embodiment of the present invention.

Fig. 2 shows one of the Pulse Control Circuits of Fig. 1.

Fig. 3 shows the other of the Pulse Control Circuits of Fig. 1.

Fig. 4 shows a possible Time Sequencing Circuit for the inverter of Fig. 1.

Fig. 5 is a timing diagram for the circuit of Fig. 4.

Fig. 6 illustrates an alternate embodiment of the inverter of Fig. 1

Fig. 7 illustrates a further alternate embodiment of the inverter of Fig. 6.

Fig. 7a shows another embodiment of the inverter of Fig. 6.

Fig. 8a and 8b illustrate waveforms for generating a sine wave output voltage.

Fig. 8c illustrates the concept for generating the waveforms of Fig. 8a.

Figs. 9a and 9b illustrate the basic concept of an integrated UPS and power supply system.

Fig. 9c shows another embodiment of an integrated UPS and power supply system.

Figs. 10 to 13 are detailed schematic circuit diagrams showing one implementation of an integrated UPS and power supply system.

Figs. 14 and 15 are detailed schematic circuit diagrams showing an implementation of an integrated UPS and power supply system of Fig. 9c.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 1 shows an inverter 10 in accordance with one embodiment of the present invention. The inverter 10 may be used in a UPS system. Inverter 10 comprises a full-bridge circuit 3 having a plurality (i.e. four) silicon controlled rectifier switches, or SCRs, S1, S2, S3, and S4, two pulse control circuits labelled 1 and 2 respectively, a time sequencing circuit 4, and a power switch circuit 5. The full bridge circuit 3 is connected directly to a positive DC input terminal 14 and is coupled through the power switch circuit 5 to a negative DC input terminal 16. Referring to Fig. 1, rectifiers S1 and S4 are positively connected in series between the DC input 14 and node 15, so that the anode of S1 is coupled to the positive DC input 14 and the cathode of S4 is connected to node 15 and is thereby coupled, through power switch circuit 5, to the negative DC input 16. As shown in Fig. 1, rectifiers S2 and S3 are similarly connected and are in parallel with the series connection of S1 and S4. The AC output voltage of the inverter is generated between terminals O1 and O2. As shown in Fig. 1, an AC load 6 is coupled between the terminals O1 and O2. Output terminal O1 is coupled to the cathode of S1 and the anode of S4, and output terminal O2 is coupled to the cathode of S2 and the anode of S3. Diode D1 is connected in parallel with S1 so that the cathode of D1 is connected to the anode of S1 and the anode of D1 is connected to the cathode of S1. Diodes D2, D3, and D4 are similarly connected in parallel across rectifiers S2, S3, and S4 respectively, as shown in Fig. 1.

The gate and cathode of SCRs S1 and S3 are connected to differential control voltage signals U1 and U3 which are generated by Pulse Control Circuit 1. Similarly, the gate and cathode of SCRs S2 and S4 are connected to differential control voltage signals U2 and U4 which are generated by Pulse Control Circuit 2.

As shown in Fig. 1, Time Sequencing Circuit 4 outputs three time-sequencing pulse signals: I1, a first half-cycle time sequencing pulse which is the input to Pulse Control Circuit 1; I2, a second half-cycle time sequencing pulse which is the input to Pulse Control Circuit 2; and I3, a control time sequencing pulse which is the input to power switch circuit 5. In a preferred embodiment, I3 pulses low during the time between the first and second half-cycles (see Fig. 5 which will be described shortly and which shows waveforms for the signals I1, I2, and I3 according to this embodiment). In an alternate embodiment, I3 may pulse high or low depending on whether the output voltage signal is greater or less than a reference waveform voltage signal.

Preferred embodiments of the Pulse Control Circuits 1 and 2 are shown in Figs. 2 and 3 respectively. Pulse Control Circuit 1 has two pairs of mutually isolated terminals to output the control pulse signals U1 and U3, and Pulse Control Circuit 2 has two pairs of mutually isolated terminals to output the control pulse signals U2 and U4.

Referring to Fig. 2, pulse transformer T1 has one primary winding and two secondary windings, with the polarity marked terminal of the primary winding connected to a reference voltage +Vf and the other terminal of the primary winding connected to the collector of transistor Q1. Note that transformer T1 need not comprise an iron core transformer. The emitter of transistor Q1 is connected to ground as is one terminal of resistor R5. The base of Q1 is connected to the other terminal of resistor R5 and to one terminal of capacitor C5. The other terminal of capacitor C5 is coupled to the input timing sequence pulse signal I1. Diode D5 is connected in series with the first secondary winding of transformer T1, and capacitor C1 and resistor R1 are each connected across the first

secondary winding of transformer T1 in the manner shown in Fig. 2. Diode D6, capacitor C3, and resistor R3 are similarly connected to the second secondary winding of transformer T1. Control pulse signal U1 is output across the terminals of C1 and R1, and control pulse signal U3 is output across the terminals of C3 and R3.

The description of the configuration of Pulse Control Circuit 2 is the same as the above description for Pulse Control Circuit 1, with components C5, R5, Q1, T1, D5, C1, R1, D6, C3, and R3 correspondingly replaced by C6, R6, Q2, T2, D7, C2, R2, D8, C4, and R4 respectively.

As shown in Fig. 1, power switch circuit 5 may comprise one power field effect transistor S5, wherein the grid or gate of S5 receives the time sequencing pulse signal I3 and thereby controls whether the channel between the source and the drain of S5, i.e. the control path, is conducting.

Fig. 4 illustrates a possible embodiment for the Time Sequencing Circuit 4 and how time sequencing pulses I1, I2, and I3 may be generated in this embodiment from the signal I0 which acts as an input to the Time Sequencing Circuit 4. As will be explained below, the signals I1, I2, and I3 may also be generated by a programmable microprocessor. This could also be achieved by a pulse current supply (not shown) as will be clear to those skilled in the art. Referring to Fig. 4, circuit 20 generates complementary high/low signals 28 and 30 which are inverted (by conventional means not shown) every half cycle of I0. Circuit 20 may comprise a flip flop triggered by I0, or alternatively signals 28 and 30 may be generated by a programmable microprocessor. One of the signals, signal 28, from circuit 20 and the signal I0 are inputs to NOR gate 22 which outputs I1, and the other signal 30 from circuit 20 and the signal I0 are inputs to NOR gate 24 which outputs I2. As a result, signal I1 pulses high during the first half cycle of I0, i.e the time period of t1 + t0, and signal I2 pulse high during the second half cycle of I0, i.e the time period of t2 + t0 (note that t2 = t1), so that signal I1 and signal I2 are in phase opposition (i.e. they are 180 degrees out of phase with each other) as shown in the timing diagram of Fig. 5.

Referring to Fig. 4, NOR gate 26 acts as a digital inverter which inverts the input I0 to produce pulse signal I3.

In operation, during the onset of the first half cycle of I0 power transistor S5 is turned on by the rising edge of I3, and transistor Q1 is turned on by the rising edge of I1 and conducts until the voltage at the base of Q1 discharges, at a rate determined by R5 and C5, below the base-emitter threshold voltage. During the short time that Q1 is conducting, pulses are produced on each of the secondary windings of transformer T1 which charge C1 and C3 respectively through D5 and D6 respectively to a certain voltage. When U1 and U3 reach the trigger voltage necessary to turn S1 and S3 on, the output voltage across O1 and O2 becomes positive as shown for VO1O2 in Fig. 5. At the end of period t1, power transistor S5 shuts off and effectively cuts off the entire circuit, while diodes D5 and D6 reversibly isolate the bridge circuit from any back swing of transformer T1. Once cut off, the current flowing through rectifiers S1 and S3 rapidly decreases to a value below the minimum current necessary to maintain the SCRs in a conducting state, i.e. the holding current. Once S1 and S3 switch off, the output voltage across O1 and O2 goes to zero and remains at that value until the first half cycle of I0 ends. Note that to prevent S1 and S3 from possible damage, diodes D1 and D3 form a discharge loop in case an inductive load gives rise to an inductive current during cut off of the circuit.

The load 6 has a high impedance which maintains a stable current when either of the switching device pairs S1-S3 or S2-S4 are conducting. This current through the load is greater than the holding current, which is the minimum current required to maintain the conducting SCRs in a conducting state after they have been turned on.

During the second half cycle of I0, power transistor S5 repeats the same turn on and cut off operation as just described for the first cycle, except in this case I2, and not I1, pulses high when I3 goes high. Control pulses U2 and U4 eventually reach a level which turns on rectifiers S2 and S4 (while S1 and S3 remain cut off). This causes the output voltage across

O1 and O2 to become negative as shown for VO1O2 in Fig. 5, before it returns to zero when S2 and S4 turn off shortly after I2 and I3 go low. When I3 goes high again, so does I1, and the cycle repeats. As illustrated in Fig. 5, the output voltage, VO1O2, is a two step per half cycle AC voltage signal. As will be explained below, different output waveforms, such as a sine wave, may also be produced by the inverter.

In one embodiment of the present invention which is illustrated in Fig. 6, a filter capacitor C7 is connected between output terminals O1 and O2 so that it is effectively in parallel with the load 6. The output terminals O1 and O2 are additionally coupled to the series connected terminals of S1 and S4 and the series connected terminals of S2 and S3 through inductor L1 and inductor L2 respectively. Inductors L1 and L2 and capacitor C7 thereby comprise a filter circuit which increases the duration of the rise and fall times of the output signal, thereby inhibiting high frequency components during the rising and falling edges of the output signal and consequently reducing interference with the load. In addition, inductors L1 and L2 also serve to dampen the load current so that the circuitry can be protected.

Also in Fig. 6, an alternate embodiment of the power switch circuit 5 is shown comprising the power field effect transistor S5, a second power field effect transistor S6, current limiting resistor R10, over current detecting resistor R9, gate or grid control resistor R7, gate or grid control transistor Q3, and resistor R8. Referring to Fig. 6, R10 is connected between the drain terminals of S5 and S6. The source of S6 is connected to a first terminal of R8 and a first terminal of R9, while the second terminal of R9 is connected to the negative DC voltage 16. The first terminal of R8 is also connected to the source of S5 (so that the source of S5 is connected to the source of S6) and the second terminal of R8 is connected to the base of Q3. The emitter of Q3 is connected to the negative DC voltage 16 and the collector of Q3 is connected to the gate of S5 and a first terminal of R7. The input I3 is coupled to the second terminal of R7 as well as directly to the

gate of S6. In this manner, the combination of R10, S6, and R9 form a control loop or control path for the power switch circuit 5.

In operation, the rising edge of the input pulse signal I3 simultaneously turns on power transistors S5 and S6. Resistor R9 samples the magnitude of the load current, and when the load current reaches a certain threshold magnitude, the voltage drop across R9 turns transistor Q3 on, which lowers the gate potential of power transistor S5, and in turn quickly leads to S5 shutting off. With S5 cut off, the load current shifts to flow through power transistor S6, whereby it is limited by the value of resistor R10. The above described current limiting approach, which does not entirely cut off the current loop, ensures that maximum power can be outputted while still maintaining safe operation of the circuitry.

The above approach is particularly advantageous in the case of a large capacitive load (i.e. approximately 200-400 micro-Farads), such as with a rectifying circuit comprising a large capacitor and a rectifying diode (and which is commonly connected to the input terminal of the switch source for a microcomputer). At the rising edge of the output signal, a large load capacitance effectively acts as a shorted load as it begins to charge. The current limiting function of the power switch circuitry protects the load while the load capacitor charges with the maximum output current that ensures safety and protection. Once the load capacitance has charged to the operating potential, the load current becomes too small to maintain the current sampling voltage across R9 at a value great enough to keep Q3 on. As a result, power transistor S5 turns on. With S5 on, the power consumption or dissipation in the inverter circuit is principally due to the voltage drop across the conducting SCR pair (either S1 - S3 or S2 - S4) and the voltage drop across S5, thus providing a high power efficiency. At the falling edge of I3, transistors S5 and S6 are cut off, and the inductive load current (from L1 and L2) continues to flow towards S5 so that the drain voltage of S5 rises. Diodes D1, D2, D3, and D4 provide a discharge loop for this current so that the SCR switches are protected, and energy is returned to positive DC voltage 14.

A further embodiment of the inverter circuit of the present invention is shown in Fig. 7. The inductors L1 and L2 of Fig. 6 are replaced by an inductor L3 which is connected between terminal 15 and the power switch circuit 5, as shown at terminal 17. In this embodiment, inductor L3 and capacitor C7 still comprise a filter circuit which increases the duration of the rise and fall times of the output signal, inhibiting high frequency components, and reducing interference with the load. Inductor L3 also serves to dampen the load current and thereby provide greater circuitry protection , as did inductors L1 and L2 in Fig. 6. However, inductor L3 also provides protection in case a short results from S1 and S4 simultaneously conducting or from S2 and S3 simultaneously conducting. Inductor L3 stops such a short current from increasing too rapidly, allowing (as explained above) the power switch circuit 5 to detect the high current, switch off transistor S5, and subsequently limit the current in the control path. Also in the embodiment of Fig. 7, diodes D1, D2, D3, and D4 are replaced by one feedback diode D9 which provides a discharge loop for a load current when the power switch is off.

Fig. 7a shows still another embodiment of the inverter circuit of the present invention. This embodiment includes the diode D9 of Fig. 7, the diodes D1, D2, D3, and D4 of Fig. 6, as well as a resistor R11 in series with a switch S7. The resistor R11 and switch S7 together form a discharge path for the output load capacitance (including C7) at the falling edge of the output waveform. The switch S7 turns on after the switches S1-S4, as well as the switches S5 and S6, have turned off (i.e. have stopped conducting).

It will be clear from the above description that the inverter circuit according to the present invention allows for the rise and fall times of the output waveform to be controlled. This can be accomplished by, for example, varying the value of R10 or C7 which together form a time constant for the output voltage signal. In the embodiment of Fig. 7A, the fall time could also be controlled by varying the value of R11.

This type of waveform modulation is suitable for some applications in which the input capacitance is fixed or limited to a certain range. For

example, in the case of a monitor, the input capacitance may range from about 0.1 μF to about 0.47 μF. For instance, if R10 = R11 = 1 KΩ and C7 = 0.1 μF, the rise and fall time constants range from 0.2 ms to 0.57 ms, and the rise and fall times range from about 0.5 ms to 1.5 ms (i.e. about 2.5 times the time constant). As already mentioned, longer transition times inhibit high frequency components, such as noise, and reduce interference with the load.

As previously mentioned, it is also possible for the inverter of the present invention to generate an output waveform which is a close approximation to a certain type of waveform, particularly a sine wave. Traditional methods of generating a sine wave output in a full-bridge inverter involve turning the four switches on and off at a high frequency. This operation is fairly complex and results in a high switching loss.

By altering the signals from the Time Sequencing Circuit 4, the inverter according to the present invention can be used to produce a stepped or porch sine wave. In this aspect of the invention, the output voltage signal is continuously compared to a normalized or standard sine wave form signal of a certain frequency and amplitude. The I1 and I2 signals effectively pulse high during alternate half cycles of the standard wave signal: I1 pulses high and I2 remains low when the standard wave signal is positive and I2 pulses high and I1 remains low when the standard wave signal is negative (in practice there will be a very short time delay after one of these signals goes low before the other goes high). The I3 signal is essentially controlled by the principal of negative feedback. When the output voltage falls below the standard wave signal, I3 goes high turning on the power switch circuit 5 (and transistor S5). This causes the output voltage to increase, and approach the value of the standard wave signal. When the output voltage signal becomes higher than the standard signal, I3 goes low, and the output voltage decreases until it is again below the standard wave signal, and the process repeats. Fig. 8a illustrates the timing for the signals I1, I2, I3 , and the output voltage signal VO1O2. As shown in Fig. 8a, the pulses of signal I3, which turn on the power switch 5, become

narrower near the zero crossings and wider near the positive and negative peaks of the output signal.

This method of output sine wave generation can be performed by a microprocessor which possesses an analog-to-digital (A/D) conversion function. Fig. 8c illustrates this concept generally. The output waveform can be sampled by a sampling circuit and A/D (conversion) port 200 in a microprocessor 202, and then compared by comparator function 206 to the numerical amplitude of the standard sine wave already stored in the microprocessor memory at 208. The microprocessor 202 (through control module 206) then generates the signals I1, I2, and I3 in response.

The present invention can also be applied to another method of generating a sine wave output voltage signal in which the inverter circuit no longer strictly converts a DC voltage to an AC voltage. In this embodiment, the voltage at terminal 14 of the inverter circuit (or alternatively at terminal 16) is not a DC signal but resembles a fully rectified half sine wave signal, as shown in Fig. 8b. The signal at terminal 16 (or alternatively at terminal 14) remains a DC signal, and preferably is at ground level. It is again necessary, in this embodiment, to compare the output voltage to a standard wave form signal. A high power converter which is controlled by a microprocessor generates the voltage signal at terminal 14. In a well known manner similar to that just described for the method illustrated by Fig. 8a, the output of the high power converter is altered, in response to the results of this comparison, to more closely resemble a half or rectified sine wave voltage signal. The signals I1, I2, and I3 may be generated as illustrated in Fig. 5, however t0, the time during which the power switch is shut off, is preferably very short in comparison with t1 and t2.

Note that both of these methods can be applied to generate signal waveforms of other shapes, for example triangular waves.

It should be noted that the use of thyristors or silicon controlled rectifier (SCR) switches S1-S4 in the bridge circuit 3 provides for several advantages over a bridge having other types of switches such as transistors.

These advantages include higher power efficiency, smaller volume/size, and lower cost. An SCR bridge circuit while advantageous in these respects over bridges containing transistor type switches, still needs to overcome certain drawbacks relating to SCRs.

First, in comparison to transistors, for switching purposes SCRs are essentially low speed or low frequency devices. In the inverter which forms part of the present invention, the addition of the power switch 5, however, allows the current through the load 6 to be switched on and cut off, independently from the SCRs S1-S4, at a much higher rate than if the SCRs had to be turned off directly. In this manner, the power switch eliminates the need to turn off a conducting SCR by, for example, connecting its gate and cathode. As discussed further below, this affords the benefits of high speed switching to the inverter circuit 10.

Second, although the SCRs S1-S4 require accurate control circuitry for switching on/off safely and simultaneously, this is again accomplished by the power switch circuit 5 which controls turn-on and cut-off of the entire bridge and ensures safe and reliable operation of the inverter 10, by avoiding both overloading and shorting of the SCRs.

Thus, unlike prior art inverter circuits which comprise transistors, the inverter of the present invention is capable of driving the SCRs S1-S4 (which require a narrow, well-defined pulse to switch on) and to permit their safe and reliable operation. The SCRs S1-S4 also provide the benefit that, once turned on, they remain in their conducting state until the current through them drops below a certain threshold. Thus there is no need for a continuously applied driving signal to maintain the SCRs in a conductive state. The removal of this requirement reduces the complexity of the Pulse Control Circuits 1 and 2 of the present invention in comparison to prior art transistor based inverter circuits.

The use of the power switch 5 is also highly advantageous with respect to waveform modulation of the AC output of the inverter. Waveform modulation is typically a requirement for inverter circuits, and is usually performed to approximate a sine wave, as described above. In

such cases, the AC output of the inverter requires low pass filtering, as effected, for example, by the elements C7 and L1 and L2 in Fig. 6. In the present invention, greatly improved waveform modulation of the AC output is achieved by rapidly turning the power switch on and off at a rate much faster than the commutation rate of the SCR switches themselves. As a result, the inductor and capacitor which comprise the low pass filter for the AC output can be made much smaller, because the required cutoff frequency of the low pass filter is much higher. In addition, the transformers T1 and T2 which isolate the bridge circuit 3 from the pulse control circuits 1, 2 can also be made much smaller and less heavy because the transformers are only required to output very narrow pulse signals to turn the SCRs on. Therefore, the power switch 5 of the present invention permits the inverter circuit 10 to be much smaller in size and weight. This is in addition to the reduction in size and weight already obtained by using SCRs (S1-S4) as the switching elements instead of transistor type switches, as in the prior art. This capability for high speed switching, despite using switches (i.e. SCRs) which are not themselves normally capable of high speed switching, permits the inverter 10 which forms part of the present invention to be of very small size and relatively low cost.

As just described, the inverter circuit according to the present invention does not comprise an iron core transformer and is capable of being designed so that its size and weight are compatible for use in small type UPS systems. Safe and reliable inverter operation is not compromised since the power switch circuit 5 acts to protect the entire system. The reduction in size of the UPS system further allows it to be conveniently integrated or merged physically with any conventional switch power supply, such as a PS/2 supply commonly used for personal computers. The UPS system according to the present invention is small and compact enough to be fitted into the power supply housing for the device itself. This is particularly beneficial, in terms of the design and portability of the device, for UPS systems which provide at least partial on-line protection and which must be at least partly connected between the utility power line

and the load. This concept is illustrated, by way of example, in Fig. 9a which shows an integrated UPS and power supply system 50 (the modules of which are shown Fig. 9b) for a computer system 210 with a peripheral monitor 64. The circuitry for the UPS system, including an inverter according to the present invention, can be physically combined on the same board 51 as the circuitry for the power supply. For example, the housing of an integrated system 50 according to the present invention can be of a size: 150 millimetres in length by 150 millimetres in width by 85 millimetres in height (and with a printed circuit board 144 mm x 105 mm x 30 mm in size). This type of integration would not be possible for prior art UPS systems comprising inverters which use iron core transformers, without significantly increasing the size of the integrated device. It should also be noted that, although the integrated system 50 can be conveniently installed in or on an electronic device, in some instance it may be preferable to make the system 50 externally connectable, for instance when the power capacity of a device is high and correspondingly a large battery is needed in the UPS circuit.

Fig. 9b shows a block diagram which illustrates the basic concept of an integrated UPS and power supply system 50 designed to protect a personal computer system. The UPS system 52 generally comprises a relay 54, a battery charger 56, battery 58 (which may be 12 V battery suitable for a personal computer), a DC/DC converter 60, and an inverter 10 in accordance with the present invention. The power supply 62 principally comprises an AC/DC converter 65 and a DC/DC converter 66. The UPS system is connected through the relay 54 between the utility power line 70 and the load 64, which, in this particular case, comprises a computer monitor.

As shown in Fig. 9b, the integrated system continuously converts AC to DC power to continuously provide the computer with clean regulated DC voltage signals. The integrated system of Fig. 9a provides double conversion to both ±5 volts DC and ±12 volts DC. This form of on-line protection results in essentially a zero transfer time in the event of

some sort of utility power failure or disruption. In the illustrated embodiment of Fig. 9b, the monitor is not backed up by on-line protection (this is not necessary since the transfer time of a few milliseconds, the switching time of the relay, is not visually perceptible to a human user). However, in an alternate embodiment the integrated system may provide complete on-line protection for a computer system or other electronic device.

Fig. 9c shows another embodiment of the present invention comprising an integrated UPS and ATX computer motherboard power supply system. As is known in the art, a PS-ON signal 90 from the motherboard (not shown) of the computer controls the normal DC output from 66 to allow for energy savings. A 5 V standby (SB) output 92 from DC/DC converter 67 is used to support various communication functions of the microcomputer, such as Wake on LAN, Wake on modem, soft power control, and so on. The converter 67 generates the standby output voltage 92 and the battery charger input voltage 94 as long as the integrated system is connected to the AC line 70.

Also in Fig. 9c the DC/DC converter 60 has two outputs 96 and 98. The output 96 supplies the voltage VDC to the DC/DC converter 66, and the output 98 supplies the voltage VD or VDC/2 to the node between capacitors 68' and 68''. A 220/110 AC Volt selector 59 determines whether the input to the inverter circuit 10 is VDC or VDC/2.

Figs. 10 to 13 are schematic circuit diagrams showing a detailed implementation for the integrated UPS and power switch supply system 50 of Fig. 9b. The operation of Figs 10 to 13 will be well understood by those skilled in the art, and so these are described only briefly here. Fig. 12 shows the control block (including timing control) of the system comprising a microprocessor module 80. Fig. 13 shows the pulse control circuits 1 and 2 and the full-bridge circuit 3 of the inverter 10. Fig. 10 shows the remainder of the integrated UPS and power supply system including a standard power supply circuit 62, relay 54, converter 60, battery charger (voltage regulator) 56, and a 12 V battery 58. Fig. 10 also shows a circuit 74, a

connector 72, and a buzzer device 76. Circuit 74 is an optional circuit designed to control the falling edge of the output signal, but which otherwise does not affect operation. Fig. 11 is a block diagram showing how Fig. 12, Fig. 13 and the connector 72 of Fig. 10 interconnect.

Similarly, Figs. 14 and 15 are schematic circuit diagrams showing a detailed implementation for the integrated UPS and power switch supply system 50 of Fig. 9c.

The microprocessor increases and monitors overall performance of the inverter and battery. It also manages power consumption, temperature and output voltage. When the system 50 is connected to a computer the microprocessor enables the system to communicate with the computer, and it can also be programmed to protect all unsaved data before automatically shutting down the computer safely. In one embodiment, the microprocessor also activates a continuous alarm when battery power is in use by sending an appropriate signal to the buzzer device 76. As the battery power becomes weaker the pitch of the alarm can be increased to inform the user to shut down the computer.

While preferred embodiments of the present invention have been described, the embodiments disclosed are illustrative and not restrictive, and the scope of the invention is intended to be defined only by the appended claims.

I CLAIM:

1. An inverter circuit (10) for converting a DC voltage between a first DC input (14) and a second DC input (16) into an AC voltage having first and second half cycles of opposite polarity across a load (6), said load (6) being coupled between a first output terminal (O1) and a second output terminal (O2), said inverter circuit (10) comprising

(a) a bridge circuit (3) comprising a plurality of silicon controlled rectifier switches (S1, S2, S3, S4) arranged in a bridge configuration, said bridge circuit being coupled between said first DC input (14) and a first node (15), said bridge circuit further being coupled to said first output terminal (O1) and said second output terminal (O2);

(b) a first pulse control circuit (1) responsive to a first pulse signal (I1) and coupled to said bridge circuit (3) for turning on a first portion (S1, S3) of said bridge circuit (3);

(c) a second pulse control circuit (2) responsive to a second pulse signal (I2) and coupled to said bridge circuit (3) for turning on a second portion (S2, S4) of said bridge circuit (3); and

(d) a timing circuit (4) coupled to said first and second pulse control circuits (1, 2) for generating the first pulse signal (I1) for controlling said first pulse control circuit (1) and the second pulse signal (I2) for controlling said second pulse control circuit (2), the first pulse signal and the second pulse signal being in phase opposition,

characterized in that:

(e) the inverter circuit (1) further comprises a power switch circuit (5) responsive to a third pulse signal (I3) and coupled between said first node (15) and said second DC input (16); and

(f) the timing circuit (4) is further coupled to the power switch circuit (5) and generates the third pulse signal (I3) for controlling the power switch circuit (5).

2. An inverter according to claim 1 characterized in that said bridge circuit comprises first, second, third, and fourth silicon controlled rectifier switches (S1, S2, S3, S4), said first silicon controlled rectifier switch (S1) being coupled between said first DC input (14) and said first output terminal (O1), said second silicon controlled rectifier switch (S2) being coupled between said first DC input (14) and said second output terminal (O2), said third silicon controlled rectifier switch (S3) being coupled between said first node (15) and said second output terminal (O2), and said fourth silicon controlled rectifier switch (S4) being coupled between said first node (15) and said first output terminal (O1).

3. An inverter according to claim 2 characterized in that said first portion of said bridge circuit comprises said first silicon controlled rectifier switch (S1) and said third silicon controlled rectifier switch (S3), and said second portion of said bridge comprises said second silicon controlled rectifier switch (S2) and said fourth silicon controlled rectifier switch (S4).

4. An inverter according to claim 3 characterized in that the anode of said first silicon controlled rectifier switch (S1) and the anode of said second silicon controlled rectifier switch (S2) are each connected to said first DC input (14), the anode of said third silicon controlled rectifier switch (S3) is connected to said second output terminal (O2), and the anode of said fourth silicon controlled rectifier switch (S4) is connected to said first output terminal (O1).

5. An inverter (10) according to claim 3 characterized in that said inverter includes an inductance (L3) coupled between the first node (15) and the power switch circuit (5).

6. An inverter according to claim 5 characterized in that said inverter includes a feedback diode (D9) having a first terminal (17) coupled to said power switch circuit (5) and a second terminal coupled to said first DC input (14).

7. An inverter according to claim 5 or 6 characterized in that the inverter further comprises a disharge path coupled between the first terminal (17) of said feedback diode (D9) and the first DC input (14), said discharge path comprising a switch (S7) and a resistance (R11), the switch (S7) being on when the silicon controlled rectifer switches (S1, S2, S3, S4) and the power switch circuit (5) are not conducting.

8. An inverter according to claim 4 or 7 characterized in that each of said first, second, third, and fourth silicon controlled rectifier switches (S1, S2, S3, S4) is connected in parallel with a diode (D1, D2, D3, D4), such that the anode of the diode is connected to the cathode of the silicon controlled rectifier and the cathode of the diode is connected to the anode of the silicon controlled rectifier.

9. An inverter according to claim 3 characterized in that said first output terminal (O1) is coupled to said first silicon controlled rectifier switch (S1) and said fourth silicon controlled rectifier switch (S4) through a first inductor (L1) and said second output terminal (O2) is coupled to said second silicon controlled rectifier switch (S2) and said third silicon controlled rectifier switch (S3) through a second inductor (L2).

10. An inverter according to claim 3, 5, or 9 characterized in that a capacitor (C7) is coupled between said first output terminal (O1) and said second output terminal (O2).

11. An inverter according to claim 3, characterized in that each of said first pulse control circuit (1) and said second pulse control circuit (2) comprises a transformer (T1, T2) having one primary winding with first and second terminals, a first secondary winding with first and second terminals, and a second secondary winding with first and second terminals, such that:

the first terminal of said primary winding is connected to a first reference signal, the second terminal of said primary winding is coupled through a switching circuit (Q1, C5, R5, Q2, C6, R6) to a second reference signal, said switching circuit being responsive to a pulse (I1, I2) signal for generating a pulse of a first polarity across said primary winding;

the first terminal of said first secondary winding is connected through a first diode (D5, D7) to a first terminal of a first capacitor (C1, C2)and a first terminal of a first resistor (R1, R2) and the second terminal of said first secondary winding is connected to a second terminal of said first capacitor (C1, C2) and a second terminal of said first resistor (R1, R2), so that an output pulse (U1, U2) is generated between the first terminal and the second terminal of said first resistor (R1, R2) in response to said pulse across said primary winding; and

the first terminal of said second secondary winding is connected through a second diode (D6, D8) to a first terminal of a second capacitor (C3, C4) and a first terminal of a second resistor (R3, R4) and the second terminal of said second secondary winding is connected to a second terminal of said second capacitor (C3, C4) and a second terminal of said second resistor (R3, R4), so that an output pulse (U3, U4) is generated between the first terminal and the second terminal of said second resistor (R3, R4) in response to said pulse across said primary winding.

12. An inverter (10) according to claim 11, characterized in that said first diode (D5, D7) and said second diode (D6, D8) are configured to isolate said first secondary winding from said first capacitor (C1, C2) and from said first resistor (R1, R2) and to isolate said second secondary winding from said second capacitor (C3, C4) and from said second resistor (R3, R4) when said pulse across said primary winding is not of said first polarity.

13. An inverter (10) according to claim 3, characterized in that said power switch circuit (5) comprises a power transistor (S5), the drain of said power transistor (S5) being connected to said bridge circuit (3), the source of said power transistor (S5) being connected to said second DC input (16), and the gate of said transistor (S5) being coupled to said third pulse signal (I3).

14. An inverter according to claim 3, characterized in that said power switch circuit (5) comprises:

(a) a first power transistor (S5), the drain of said first power transistor (S5) being connected to said bridge circuit (3), and the gate of said first power transistor (S5) being coupled through a first resistor (R7) to said intermittent cycle pulse signal (I3);

(b) a second power transistor (S6), the gate of said second power transistor (S6) being coupled to said intermittent cycle pulse signal (I3) and the source of said second power transistor (S6) being coupled to the source of said first power transistor (S5);

(c) a third transistor (Q3);

(d) a second resistor (R8) coupled between the source of said first power transistor (S5) and the base of said third transistor (Q3);

(e) a third resistor (R9) coupled between the source of said second power transistor (S6) and the second DC input (16) for detecting the magnitude of the current between said first

output terminal (O1) and said second output terminal (O2); and

(f) a fourth resistor (R10) coupled between the drain of said first power transistor (S5) and the drain of said second power transistor (S6) for limiting the magnitude of said current between said first output terminal (O1) and said second output terminal (O2) when said magnitude exceeds a threshold value.

15. An inverter according to claim 13 or 14, characterized in that said second DC input (16) is at a lower voltage level than said first DC input (14).

16. An inverter circuit (10) for generating an AC voltage having first and second half cycles of opposite polarity and a wave form of a certain shape, said inverter circuit (10) converting a DC voltage between a first DC input (14) and a second DC input (16) into said AC voltage across a load (6), said load (6) being coupled between a first output terminal (O1) and a second output terminal (O2), characterized in that the inverter circuit (10) comprises:

(a) a bridge circuit (3) comprising a plurality of silicon controlled rectifier switches (S1, S2, S3, S4) arranged in a bridge configuration, said bridge circuit (3) being coupled between said first DC input (14) and a first node (15), said bridge circuit (3) further being coupled to said first output terminal (O1) and said second output terminal (O2);

(b) a power switch circuit (5) responsive to a third pulse signal (I3) and coupled between said first node (15) and said second DC input (16);

(c) a first pulse control circuit (1) responsive to a first pulse signal (I1) and coupled to said bridge circuit (3) for turning on a first portion (S1, S3) of said bridge circuit (3);

(d) a second pulse control circuit (2) responsive to a second pulse signal (I2) and coupled to said bridge circuit (3) for turning on a second portion (S2, S4) of said bridge circuit (3);

(e) a timing circuit (4) coupled to said first and second pulse control circuits (1, 2) and to said power switch circuit (5) for generating a first pulse signal (I1) for controlling the first pulse control circuit (1), a second pulse signal (I2) for controlling the second pulse control circuit (2), the first pulse signal(I1) and the second pulse signal (I2) being in phase opposition, and a third pulse signal (I3) for controlling the power switch circuit (5);

(f) a circuit for providing a standard signal in the shape of said wave form;

(g) said inverter circuit being configured such that said first pulse signal (I1) pulses high and said second pulse signal (I2) remains low during the first half cycle of said standard signal; said second pulse signal (I2) pulses high and said first pulse signal (I1) remains low during the second half cycle of the standard signal; said third pulse signal (I3) pulses high if the value of said AC voltage is less than the value of said standard signal; and said third pulse signal (I3) remains low if the value of said AC voltage is greater than the value of said standard signal.

17. A method of using an inverter circuit (10) to generate an AC voltage having first and second half cycles of opposite polarity and a wave form of a certain shape, said inverter circuit (10) converting a DC voltage between a first DC input (14) and a second DC input (16) into said AC voltage across a load (6), said load (6) being coupled between a first output terminal (O1) and a second output terminal (O2), said inverter circuit (10) comprising:

a bridge circuit (3) comprising a plurality of silicon controlled rectifier switches (S1, S2, S3, S4) arranged in a bridge

configuration, said bridge circuit (3) being coupled between said first DC input (14) and a first node (15), said bridge circuit (3) further being coupled to said first output terminal (O1) and said second output terminal (O2);

a power switch circuit (5) responsive to a third pulse signal (I3) and coupled between said first node (15) and said second DC input (16);

a first pulse control circuit (1) responsive to a first pulse signal (I1) and coupled to said bridge circuit (3) for turning on a first portion of said bridge circuit (3);

a second pulse control circuit (2) responsive to a second pulse signal (I2) and coupled to said bridge circuit (3) for turning on a second portion (S2, S4) of said bridge circuit (3); and

a timing circuit (4) coupled to said first and second pulse control circuits (1, 2) and to said power switch circuit (5) for generating a first pulse signal (I1) for controlling said first pulse control circuit (1), a second pulse signal (I2) for controlling said second pulse control circuit (2), said first pulse signal (I1) and said second pulse signal (I2) being in phase opposition, and a third pulse signal (I3) for controlling said power switch circuit (5);

characterized in that said method comprises the steps of:

(a) providing a standard signal in the shape of said wave form;

(b) pulsing said first pulse signal (I1) high and maintaining said second pulse signal (I2) low during the first half cycle of said standard signal;

(c) pulsing said second pulse signal (I2) high and maintaining said first pulse signal (I1) low during the second half cycle of said standard signal;

(d) pulsing said third pulse signal (I3) high if the value of said AC voltage is less than the value of said standard signal; and

(e) maintaining said third pulse signal (I3) low if the value of said AC voltage is greater than the value of said standard signal.

18. A method of using an inverter circuit (10) to generate an AC voltage having first and second half cycles of opposite polarity and a wave form of a certain shape, said inverter circuit (10) converting a voltage between a first input (14) and a second input (16) into said AC voltage across a load (6), said load (6) being coupled between a first output terminal (O1) and a second output terminal (O2), said inverter circuit (10) comprising:

a bridge circuit (3) comprising a plurality of silicon controlled rectifier switches (S1, S2, S3, S4) arranged in a bridge configuration, said bridge circuit (3) being coupled between said first input (14) and a first node (15), said bridge circuit (3) further being coupled to said first output terminal (O1) and said second output terminal (O2);

a power switch circuit (5) responsive to a third pulse signal (I3) and coupled between said first node (15) and said second input (16);

a first pulse control circuit (1) responsive to a first pulse signal (I1) and coupled to said bridge circuit (3) for turning on a first portion of said bridge circuit (3);

a second pulse control circuit (2) responsive to a second pulse signal (I2) and coupled to said bridge circuit (3) for turning on a second portion (S2, S4) of said bridge circuit (3); and

a timing circuit (4) coupled to said first and second pulse control circuits (1, 2) and to said power switch circuit (5) for generating a first pulse signal (I1) for controlling said first pulse control circuit (1), a second pulse signal (I2) for controlling said second pulse control circuit (2), said first pulse signal (I1) and said second pulse signal (I2) being in

phase opposition, and a third pulse signal (I3) for controlling said power switch circuit (5);

characterized in that said method comprises the steps of:

(a) providing a standard signal in the shape of said wave form;

(b) providing a fully rectified signal at one of said first input (14) or said second input (16) and providing a DC input at the other of said first input or said second input.

(c) pulsing said first pulse signal (I1) high and maintaining said second pulse signal (I2) low during the first half cycle of said standard signal;

(d) pulsing said second pulse signal (I2) high and maintaining said first pulse (I1) signal low during the second half cycle of said standard signal;

(e) pulsing said third pulse signal (I3) low so as to turn the power switch (5) off during periods between a pulse of said first pulse signal (I1) and a pulse of said second pulse signal (I2);

(f) increasing the amplitude of said fully rectified signal if the value of said AC voltage is less than the value of said standard signal; and

(g) decreasing the amplitude of said fully rectified signal if the value of said AC voltage is greater than the value of said standard signal;

such that said fully rectified signal resembles a signal in the shape of said wave form which has been fully rectified.

19. An integrated uninterruptible power supply (UPS) and power supply system (50) for protecting a device from disruptions in utility AC power, said device having a power supply circuit (62) installed thereon for receiving utility AC power installed thereon, characterized in that said integrated UPS and power supply system comprises said power supply circuit (62) and an uninterruptible power supply system circuit (52), said uninterruptible power supply system circuit comprising a battery (58) and

an inverter circuit (10), said inverter circuit not having an iron core transformer and being of small size.

20. An integrated UPS and power supply system (50) according to claim 19 characterized in that said inverter circuit (10) of said uninterruptible power supply system converts a DC voltage between a first DC input (14) and a second DC input (16) into an AC voltage having first and second half cycles of opposite polarity across a load (6), said load (6) being coupled between a first output terminal (O1) and a second output terminal (O2), said inverter circuit comprising

(a) a bridge circuit (3) comprising a plurality of silicon controlled rectifier switches (S1, S2, S3, S4) arranged in a bridge configuration, said bridge circuit being coupled between said first DC input (14) and a first node (15), said bridge circuit further being coupled to said first output terminal (O1) and said second output terminal (O2);

(b) a power switch circuit (5) responsive to a third pulse signal (I3) and coupled between said first node (15) and said second DC input (16);

(c) a first pulse control circuit (1) responsive to a first pulse signal (I1) and coupled to said bridge circuit (3) for turning on a first portion (S1, S3) of said bridge circuit (3);

(d) a second pulse control circuit (2) responsive to a second pulse signal (I2) and coupled to said bridge circuit (3) for turning on a second portion (S2, S4) of said bridge circuit (3); and

(e) a timing circuit (4) coupled to said first and second pulse control circuits (1, 2) and to said power switch circuit (5) for generating a first pulse signal for controlling said first pulse control circuit (1) and a second pulse signal for controlling said second pulse control circuit (2), said first pulse signal and said second pulse signal being in phase opposition, and a third pulse signal for controlling said power switch circuit (5).

21. An integrated power supply system according to claim 20 characterized in that said bridge circuit (3) comprises first, second, third, and fourth silicon controlled rectifier switches (S1, S2, S3, S4), said first silicon controlled rectifier switch (S1) being coupled between said first DC input (14) and said first output terminal (O1), said second silicon controlled rectifier switch being coupled between said first DC input (14) and said second output terminal (O2), said third silicon controlled rectifier switch being coupled between said first node (15) and said second output terminal (O2), and said fourth silicon controlled rectifier switch (S4) being coupled between said first node (15) and said first output terminal (O1).

22. An integrated power supply system according to claim 21 characterized in that said first portion of said bridge circuit comprises said first silicon controlled rectifier switch (S1) and said third silicon controlled rectifier switch (S3), and said second portion of said bridge (3) comprises said second silicon controlled rectifier switch (S2) and said fourth silicon controlled rectifier switch (S4).

23. An integrated power supply system according to any of claims 19 to 22 and being installed within said device, said device being a computer.

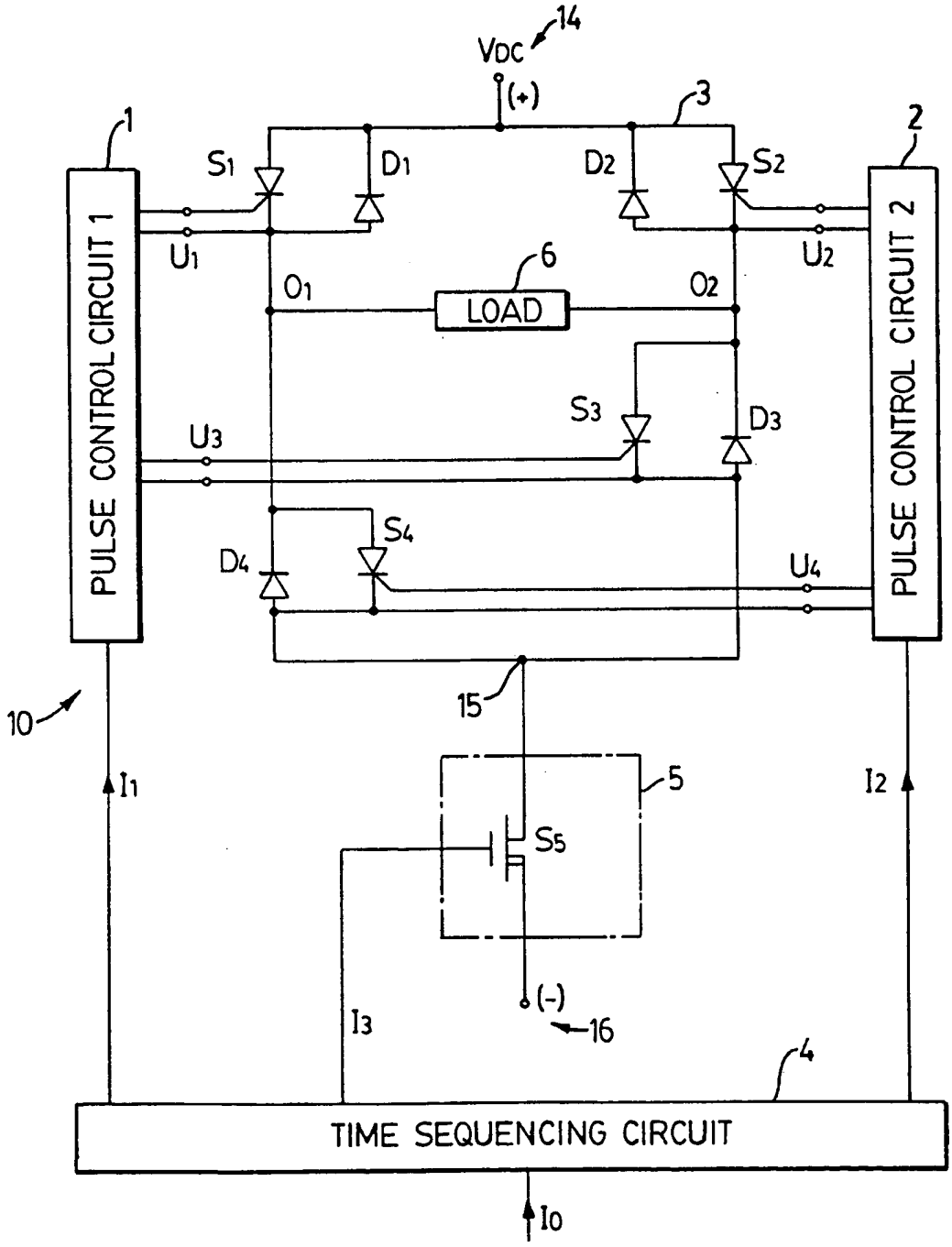

VDC
14
(+)
3
1
2
S1
D1
D2
S2
PULSE CONTROL CIRCUIT 1
PULSE CONTROL CIRCUIT 2
U1
U2
O1
6
LOAD
O2
S3
D3
U3
S4
D4
U4
15
10
I1
I2
5
S5
(-)
16
I3
4
TIME SEQUENCING CIRCUIT
I0

FIG. 1

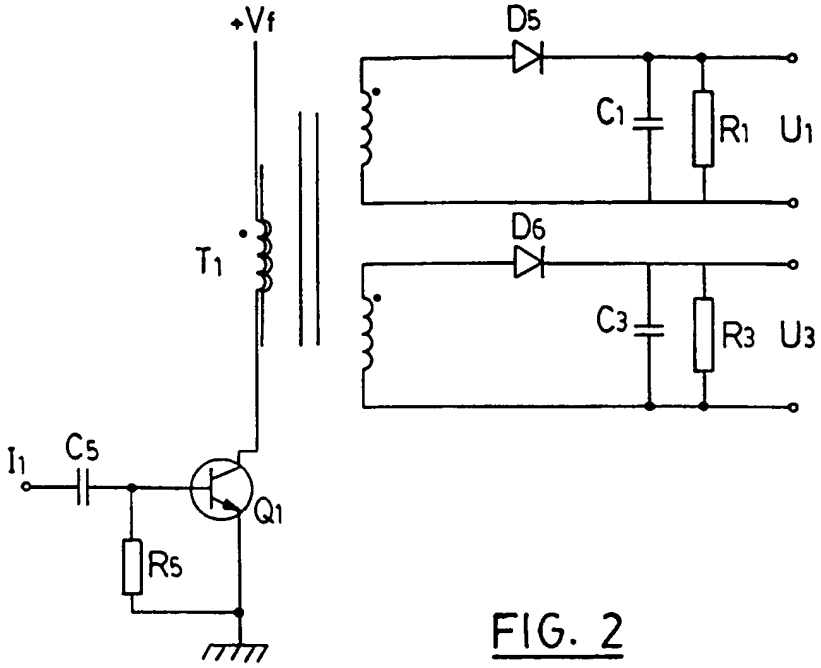

+Vf
D5
C1
R1
U1
T1
D6
C3
R3
U3
I1
C5
Q1
R5

FIG. 2

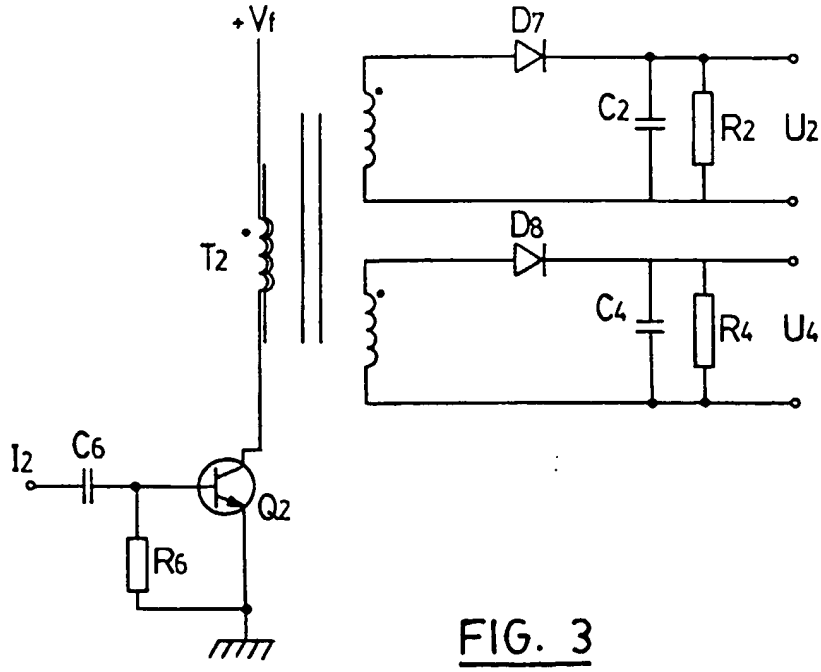

+Vf
D7
C2
R2
U2
T2
D8
C4
R4
U4
I2
C6
Q2
R6

FIG. 3

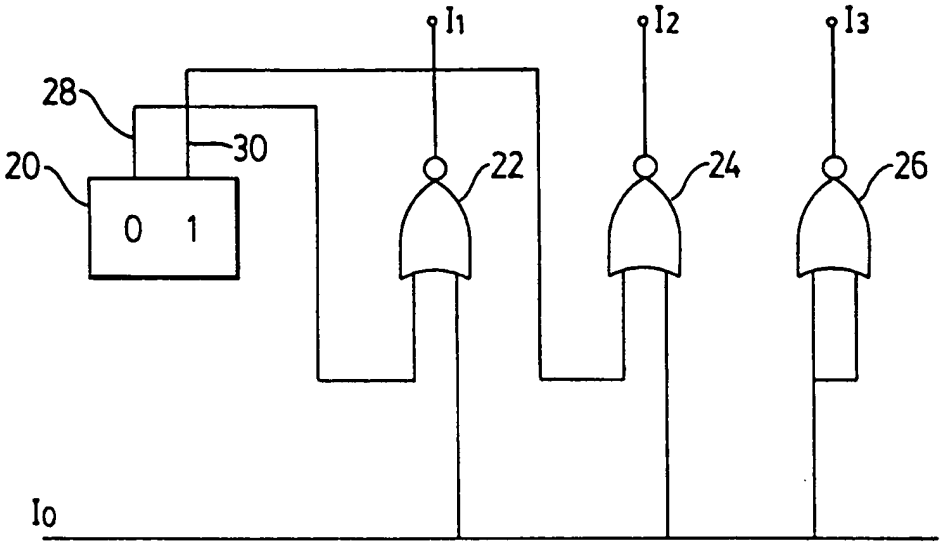

I1
I2
I3
28
30
20
0 1
22
24
26
Io

FIG. 4

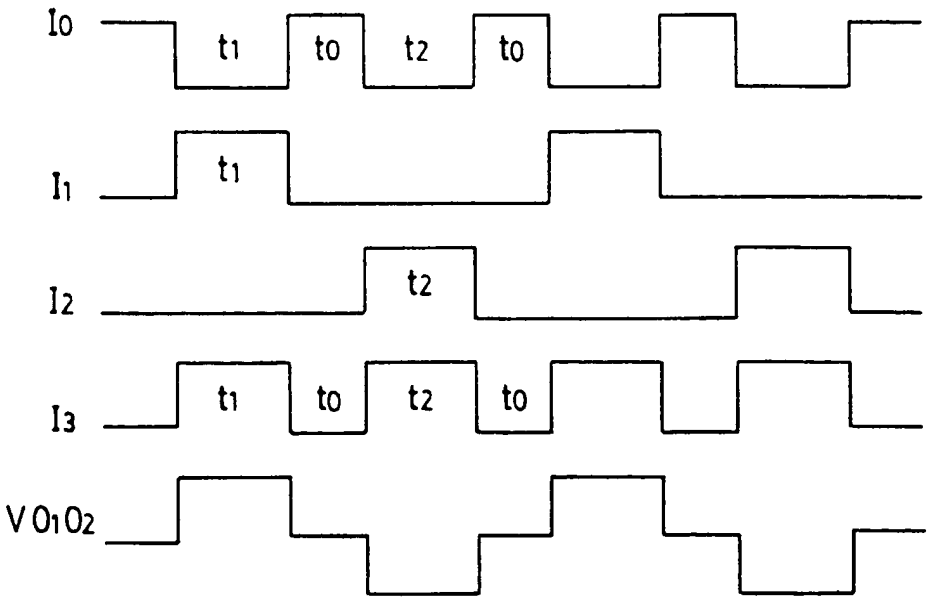

Io
t1
to
t2
to
I1
t1
I2
t2
I3
t1
to
t2
to
V O1O2

FIG. 5

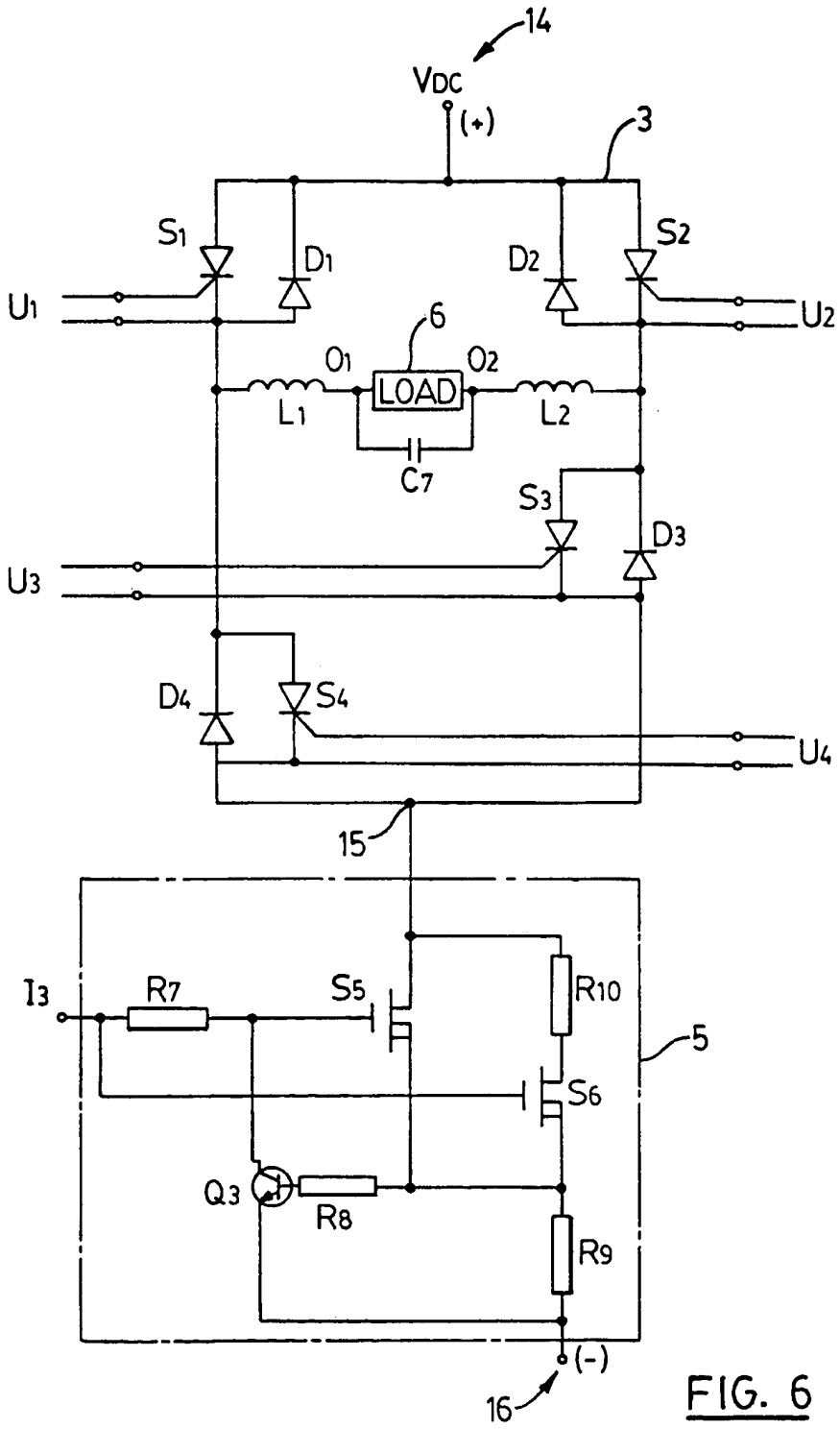

14
VDC
(+)
3
S1
D1
D2
S2
U1
U2
6
O1
O2
LOAD
L1
L2
C7
S3
D3
U3
D4
S4
U4
15
I3
R7
S5
R10
5
S6
Q3
R8
R9
(-)
16

FIG. 6

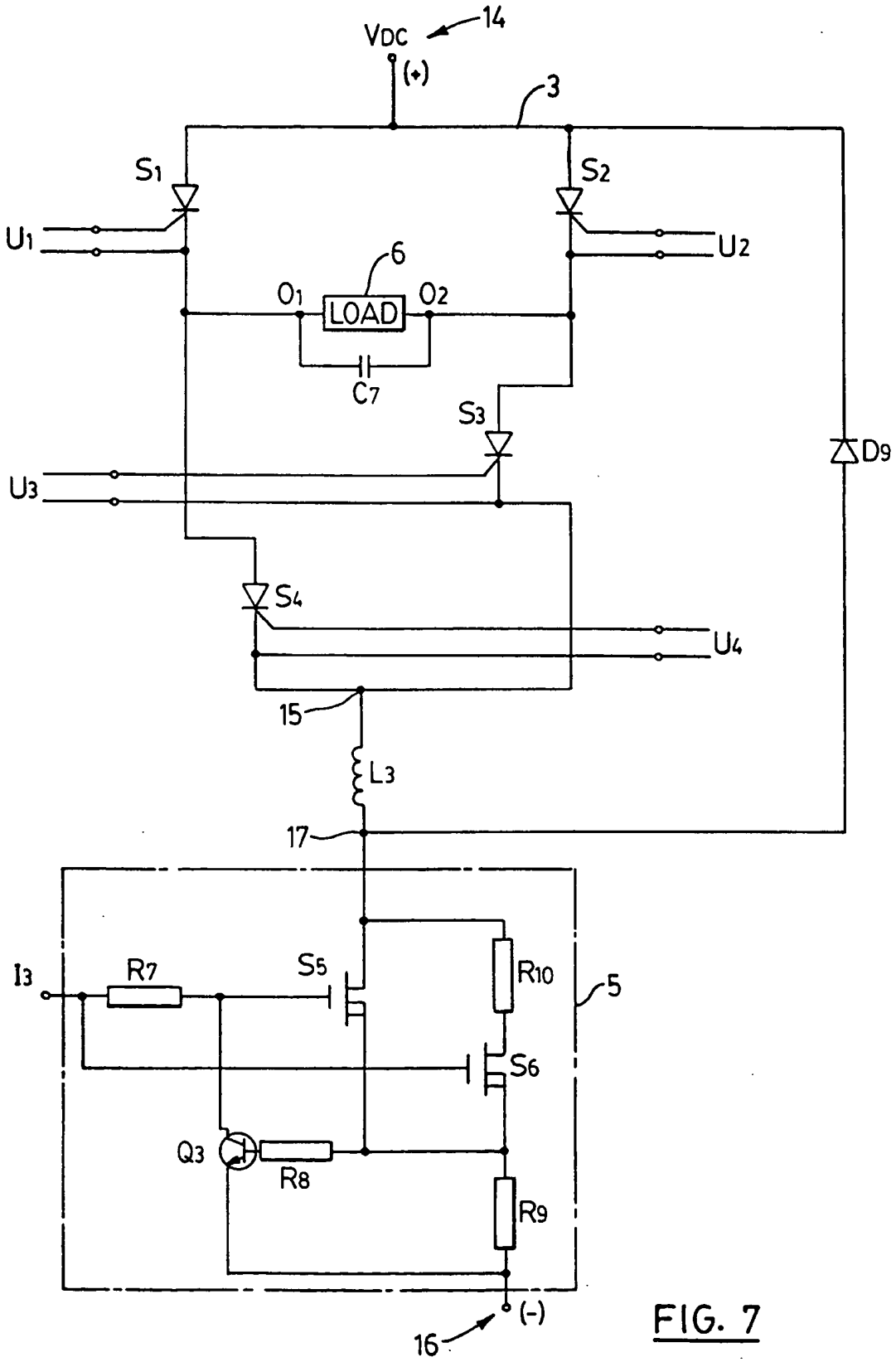

VDC
14
(+)
3
S1
S2
U1
U2
6
O1
LOAD
O2
C7
S3
D9
U3
S4
U4
15
L3
17
I3
R7
S5
R10
5
S6
Q3
R8
R9
(-)
16

FIG. 7

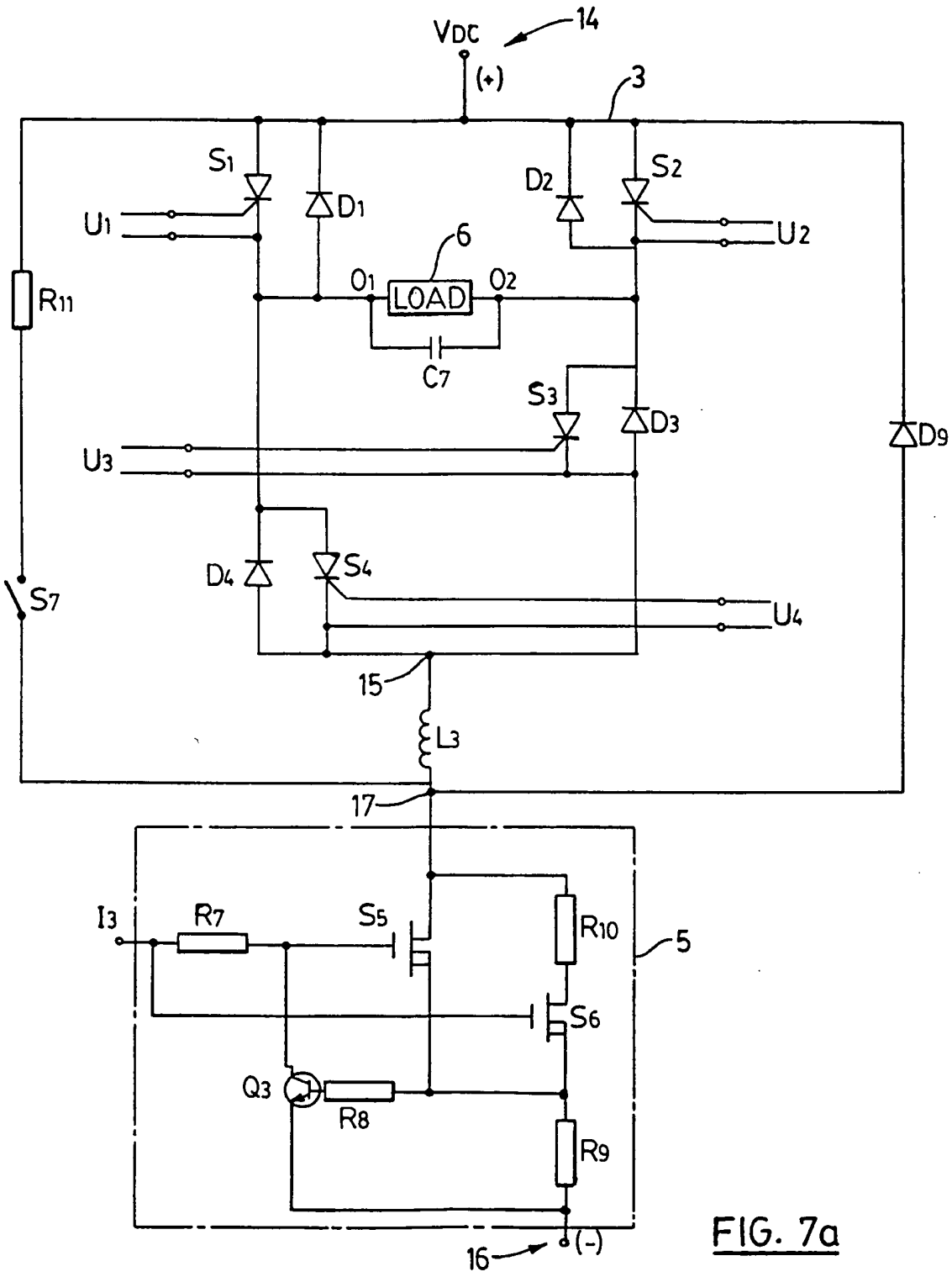

VDC
14
(+)
3
S1
D1
D2
S2
U1
U2
6
O1
LOAD
O2
R11
C7
S3
D3
D9
U3
D4
S4
S7
U4
15
L3
17
I3
R7
S5
R10
5
S6
Q3
R8
R9
16
(-)

FIG. 7a

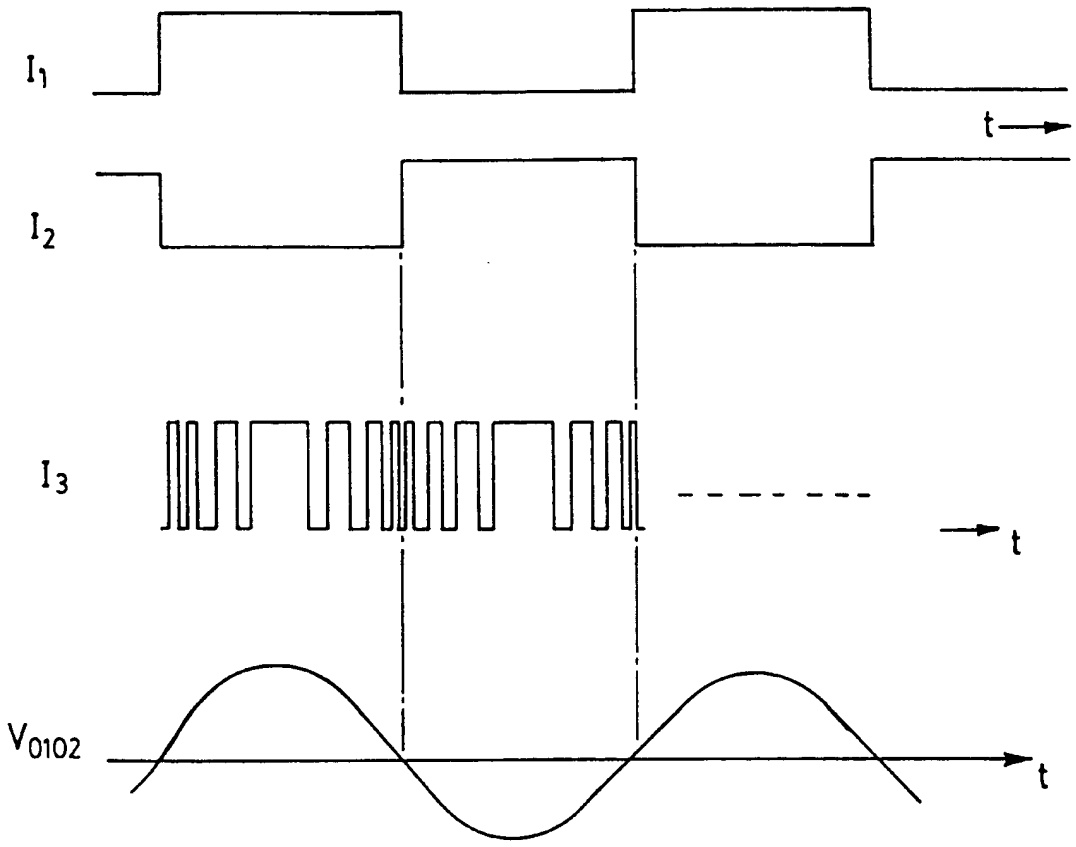


FIG. 8a

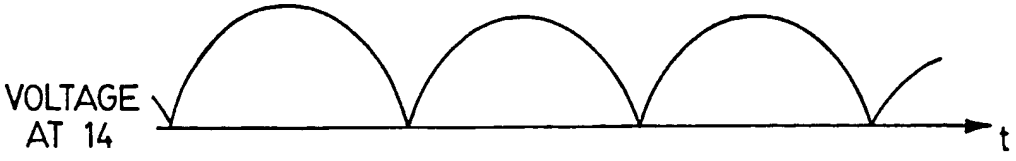


FIG. 8b

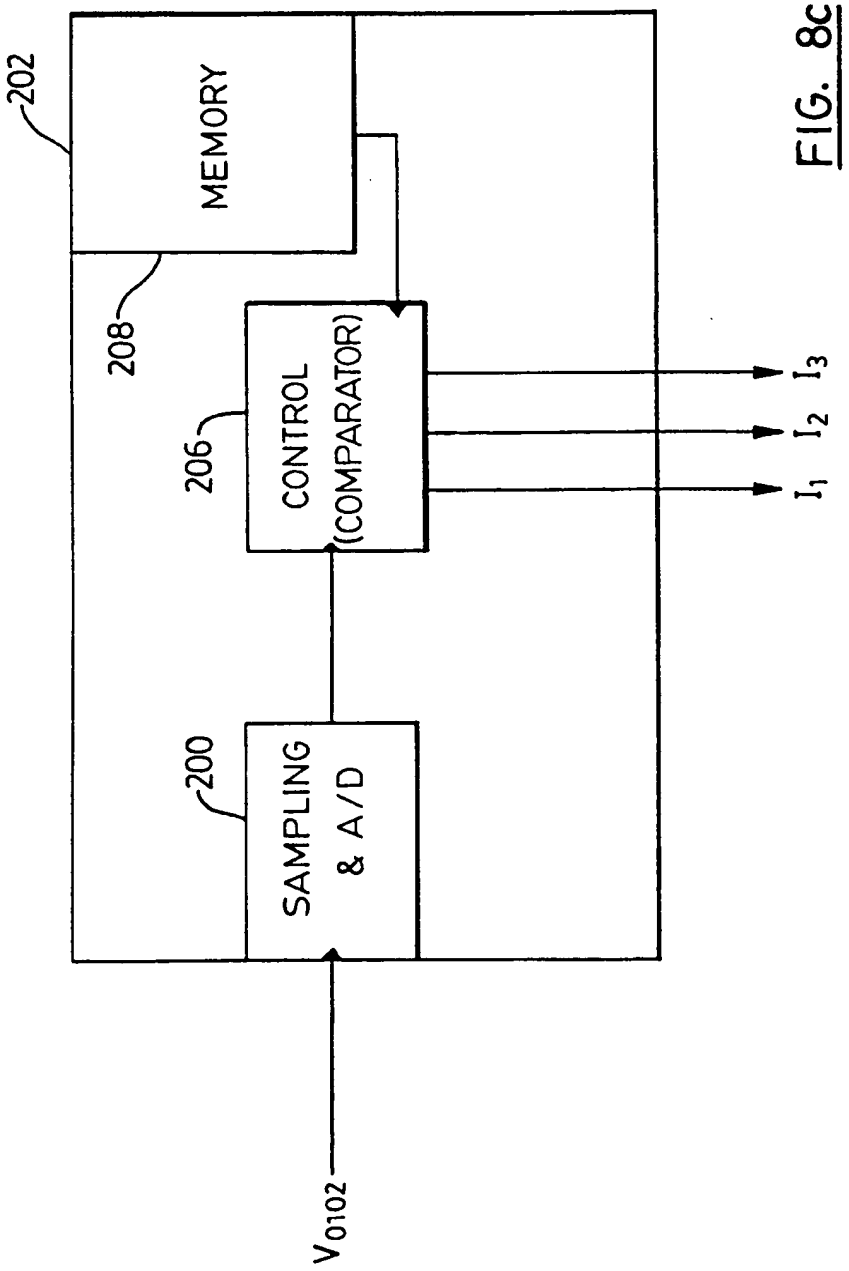

202
MEMORY
208
206
CONTROL
(COMPARATOR)
I_1 I_2 I_3
200
SAMPLING
& A/D
V_{0102}

FIG. 8c

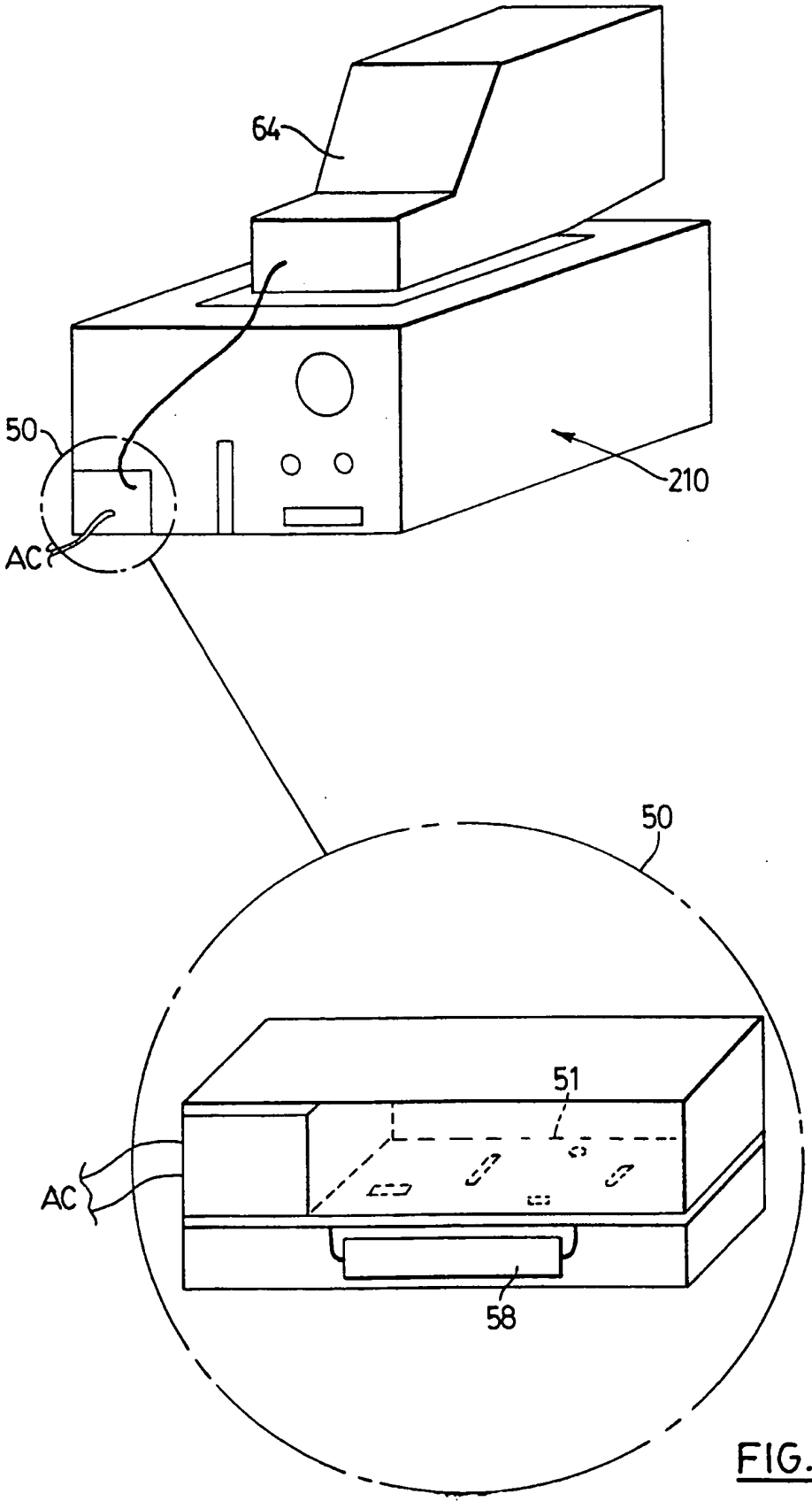
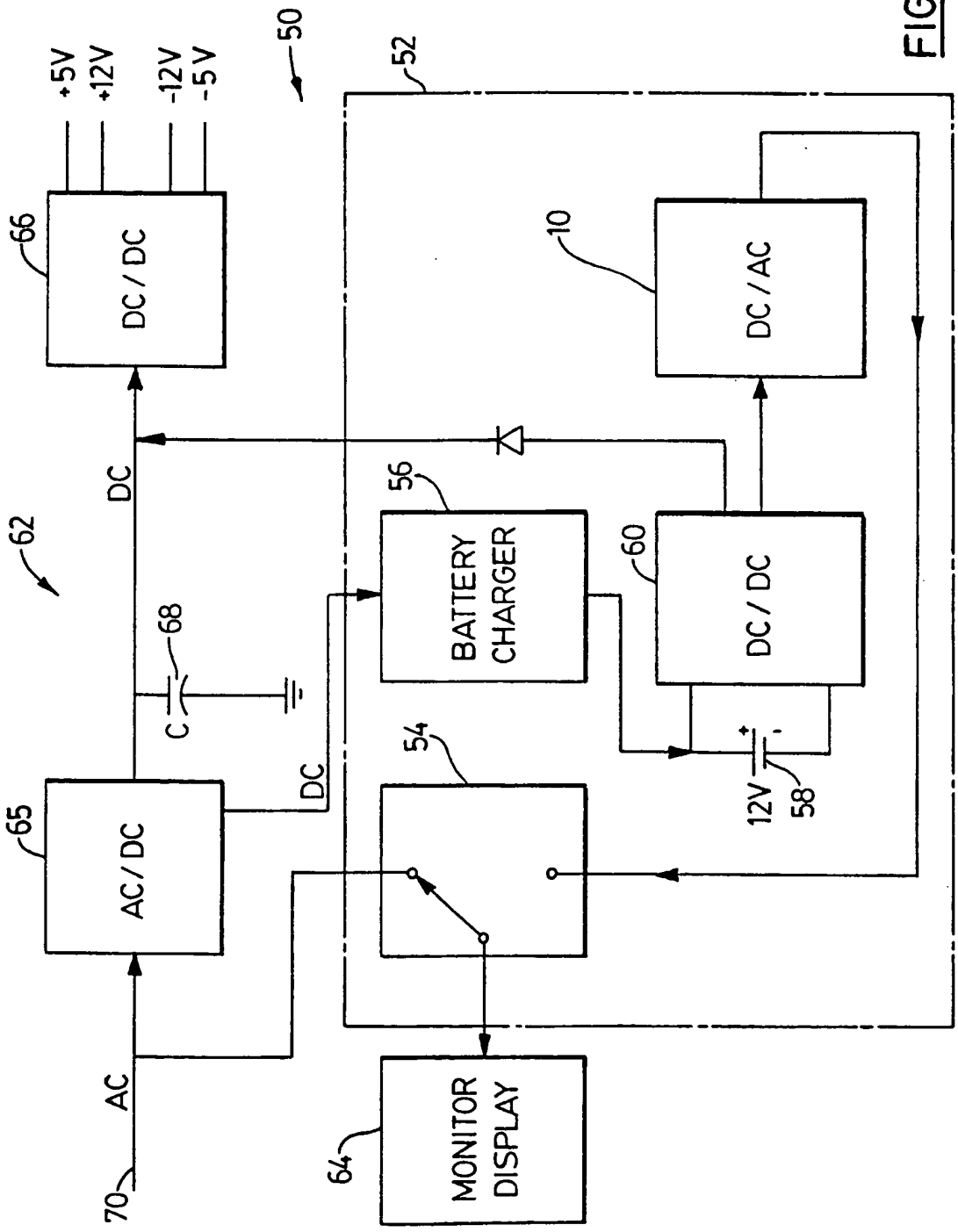


FIG. 9a

FIG. 9B


+5V
+12V
-12V
-5V
50
52
66
DC / DC
10
DC / AC
DC
56
BATTERY CHARGER
60
DC / DC
62
68
C
54
12V
58
65
AC / DC
DC
AC
70
64
MONITOR DISPLAY

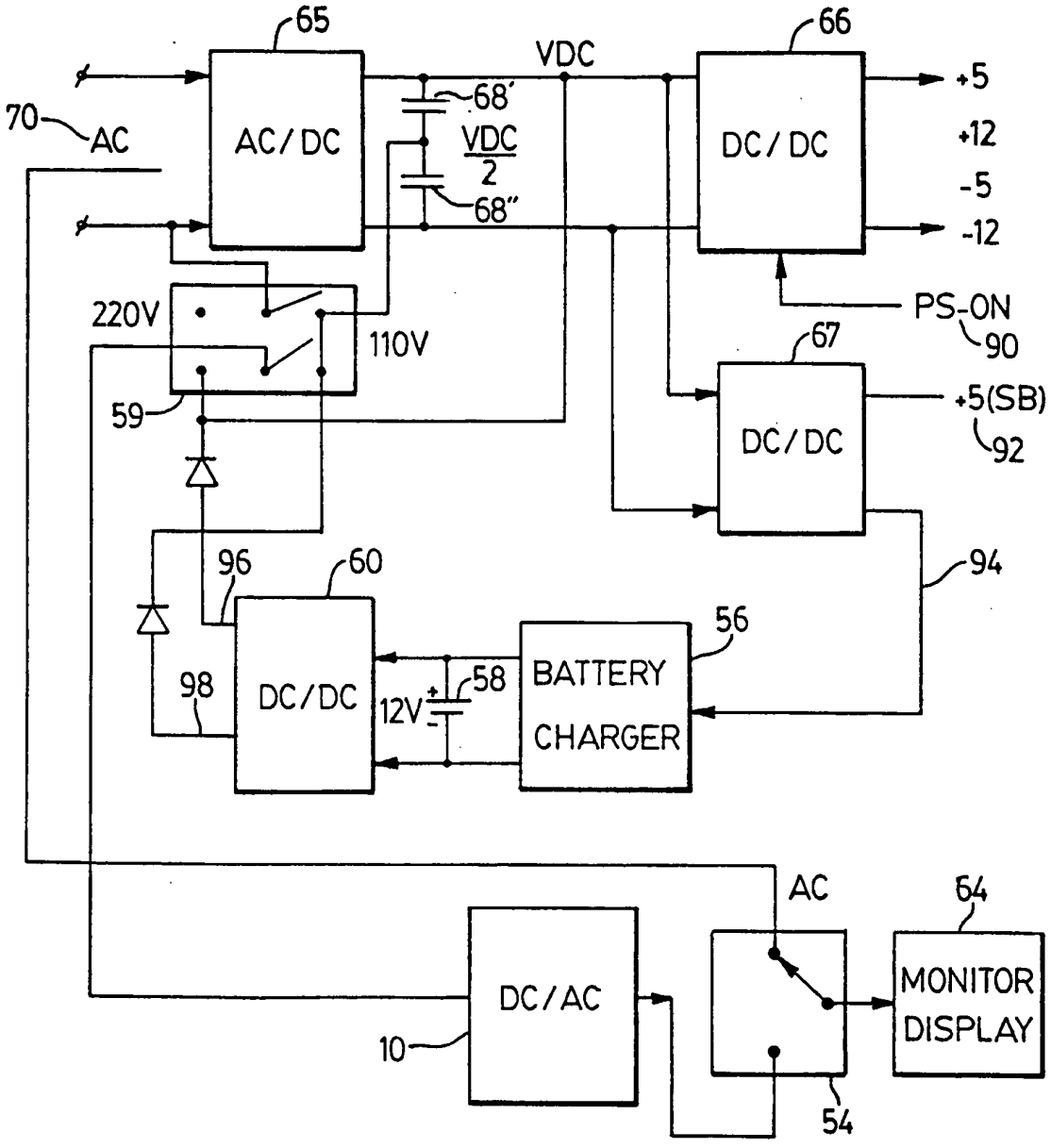

65
AC/DC
VDC
66
DC/DC
+5
+12
-5
-12
70
AC
68'
VDC
2
68"
220V
110V
PS-ON
90
67
DC/DC
+5(SB)
92
59
94
96
60
56
98
DC/DC
12V
58
BATTERY
CHARGER
AC
64
DC/AC
MONITOR
DISPLAY
10
54

FIG. 9c

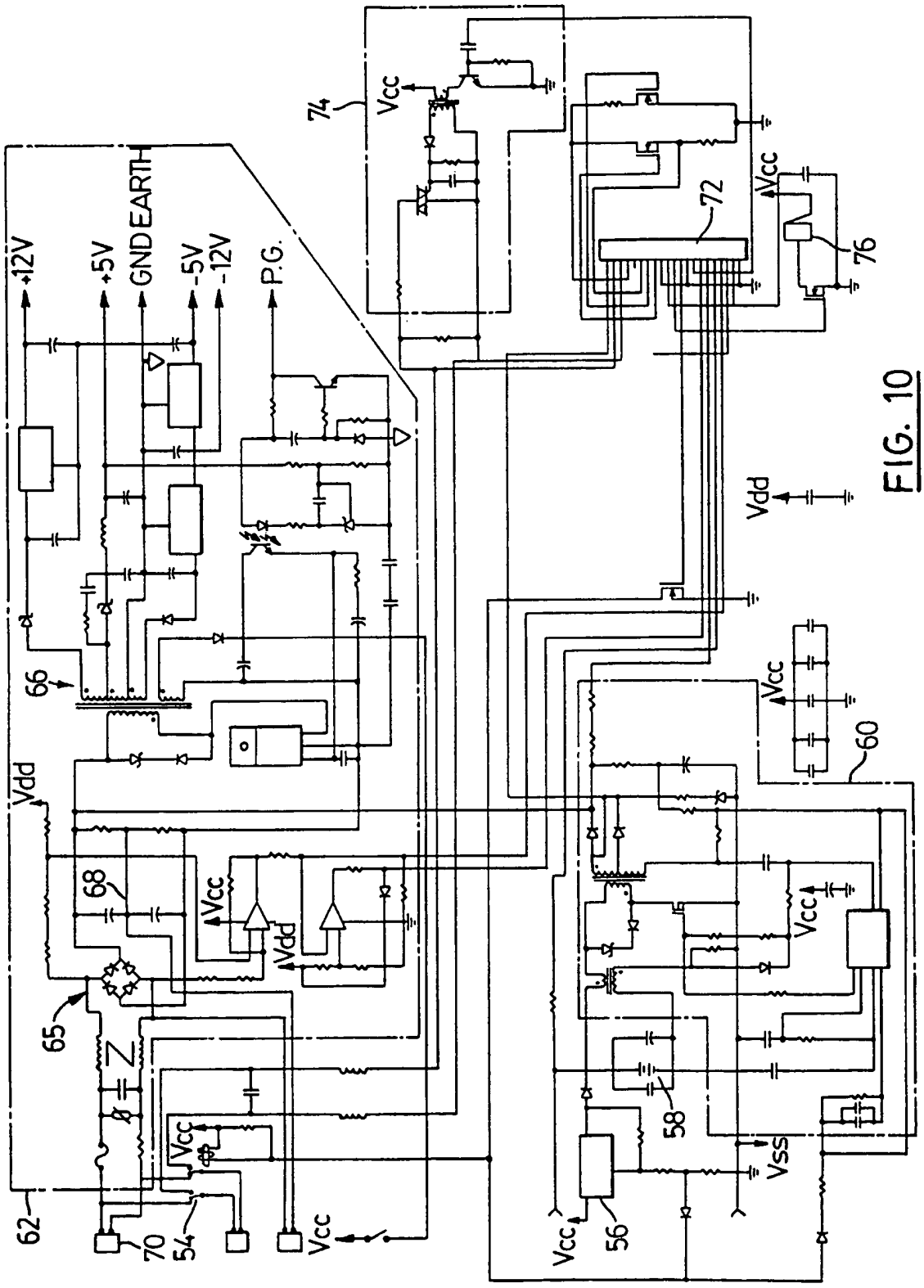

+12V
+5V
GND EARTH
-5V
-12V
P.G.
74
Vcc
72
76
66
Vdd
68
65
62
70
54
58
56
60
Vss

FIG. 10

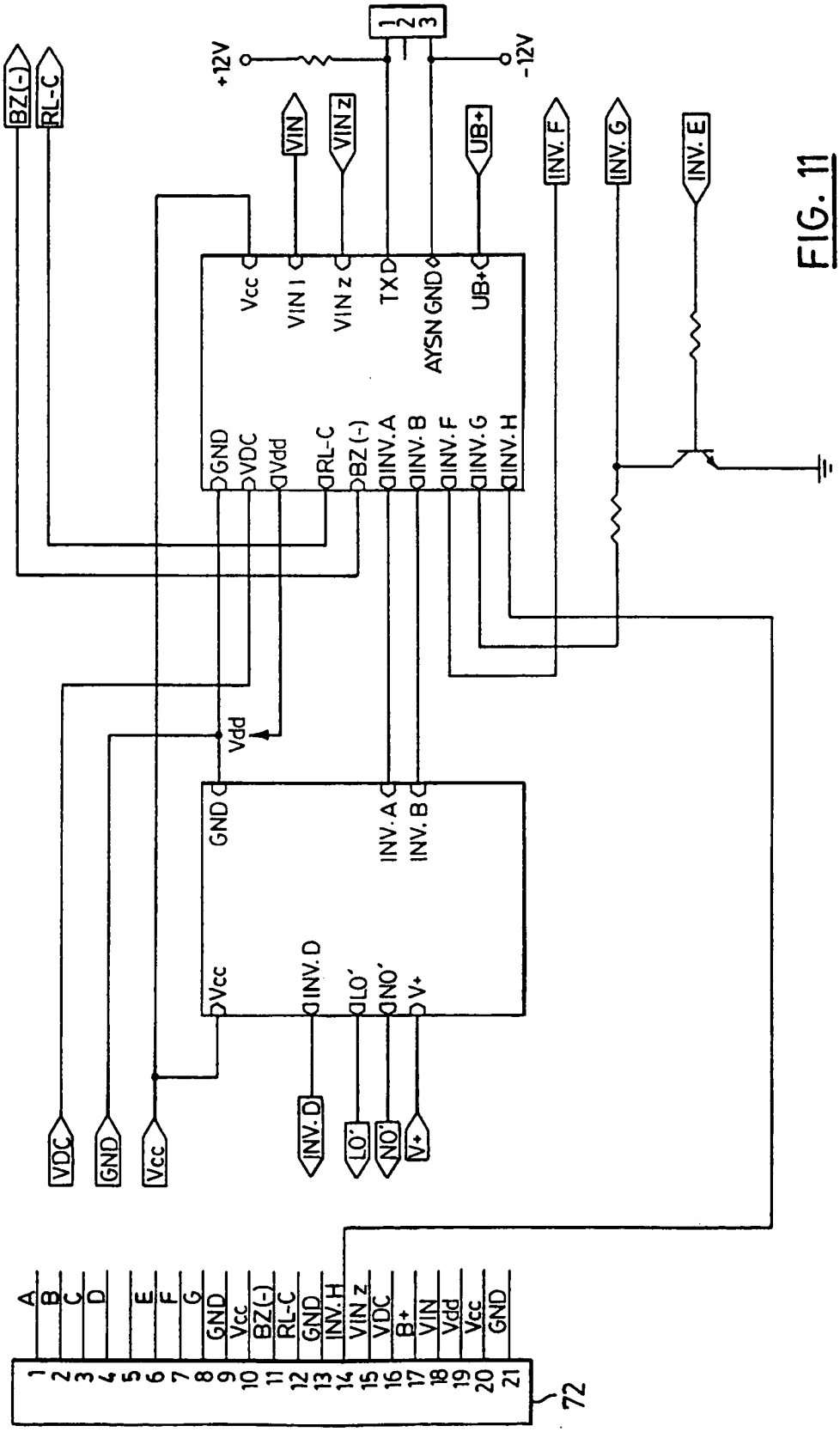

BZ(-)
RL-C
+12V
-12V
1
2
3
VIN
VIN z
UB+
INV. F
INV. G
INV. E
Vcc
VIN I
VIN z
TXD
AYSN GND
UB+
GND
VDC
Vdd
RL-C
BZ(-)
INV. A
INV. B
INV. F
INV. G
INV. H
Vdd
GND
INV. A
INV. B
Vcc
INV. D
LO'
NO'
V+
VDC
GND
Vcc
INV. D
LO'
NO'
V+
A
B
C
D
E
F
G
GND
Vcc
BZ(-)
RL-C
GND
INV. H
VIN z
VDC
B+
VIN
Vdd
Vcc
GND
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21
72

FIG. 11

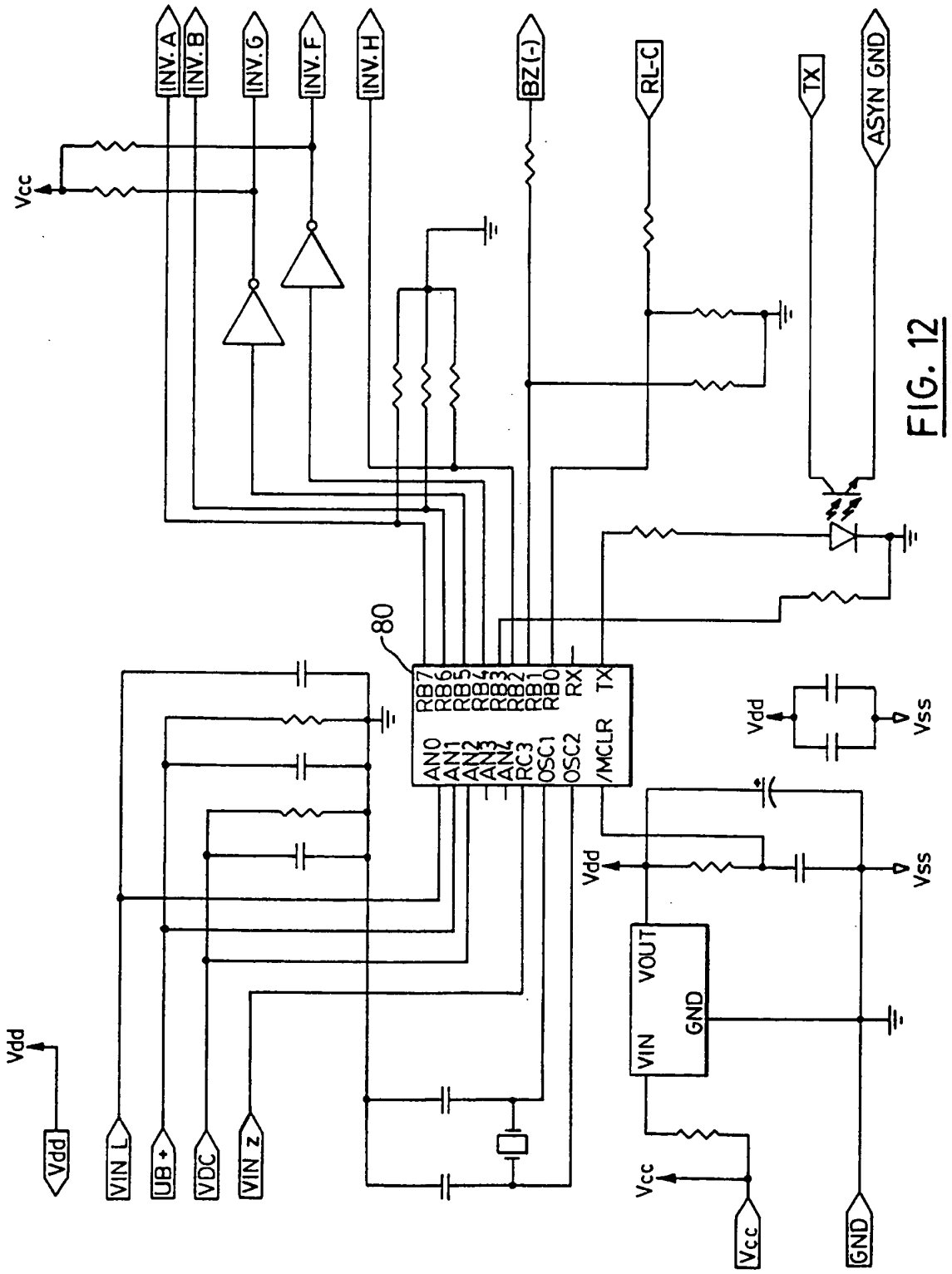

INV.A
INV.B
INV.G
INV.F
INV.H
BZ(-)
RL-C
TX
ASYN GND
Vcc
80
RB7
RB6
RB5
RB4
RB3
RB2
RB1
RB0
RX
TX
AN0
AN1
AN2
AN3
AN4
RC3
OSC1
OSC2
/MCLR
Vdd
Vss
VOUT
GND
VIN
Vdd
VIN L
UB+
VDC
VIN z
Vcc
GND

FIG. 12

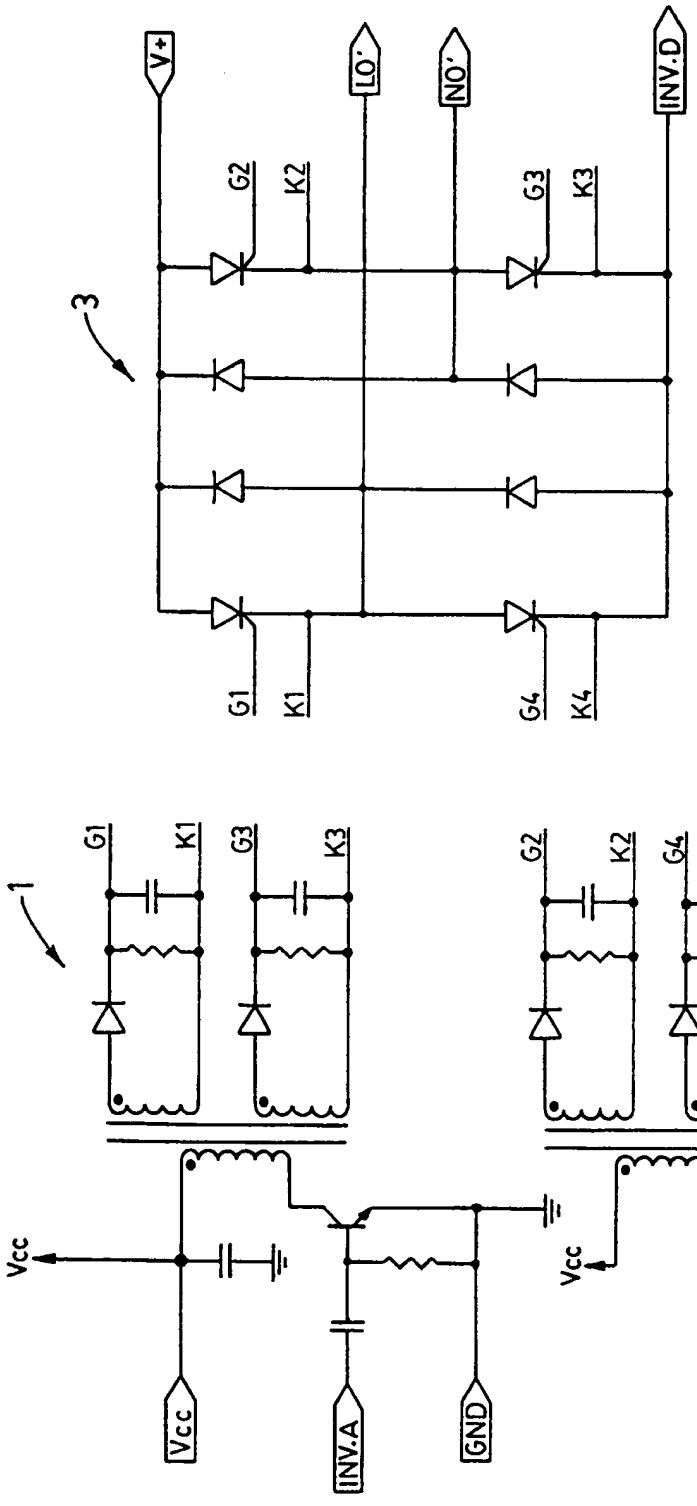


FIG. 13

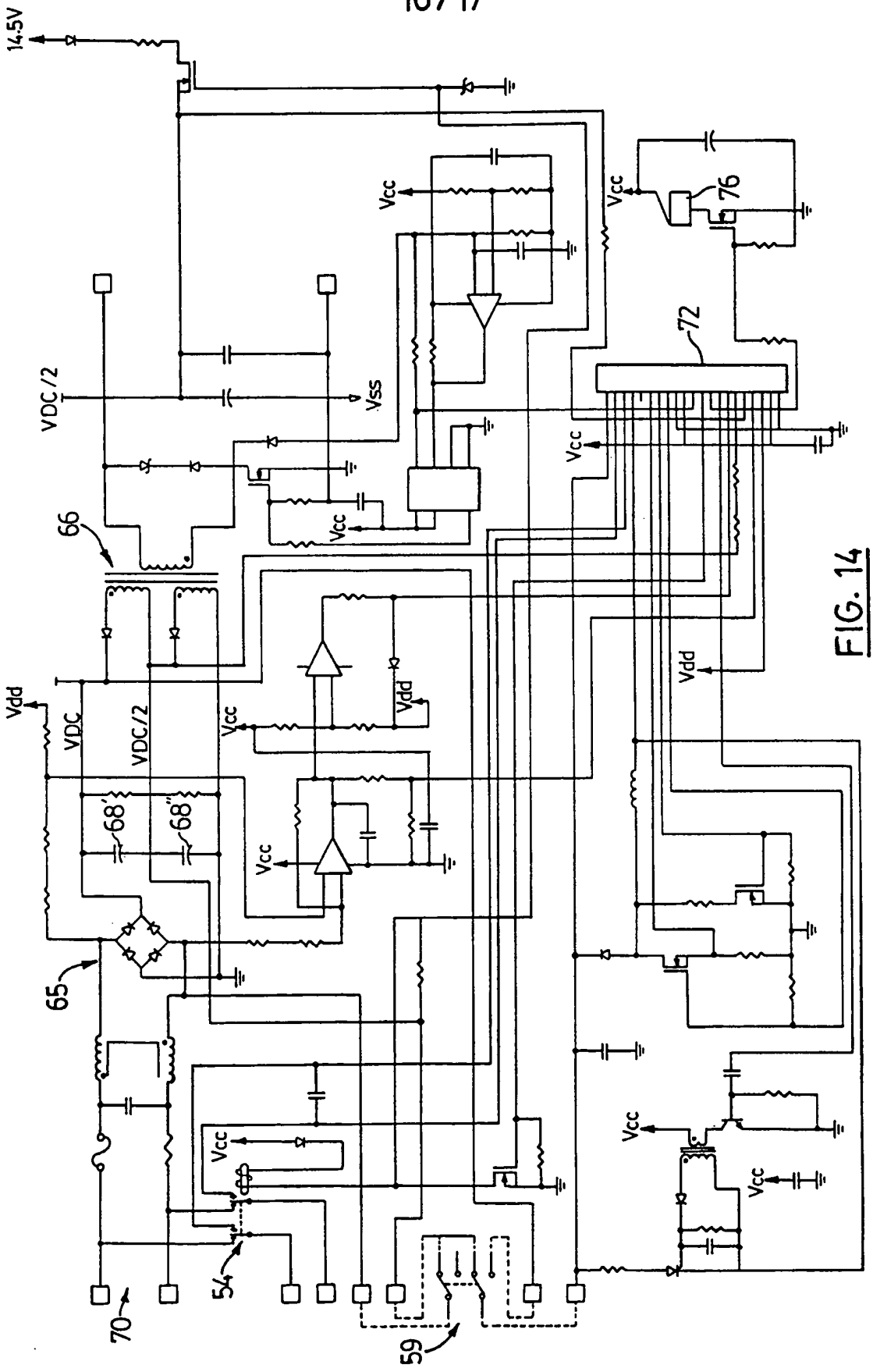


FIG. 14

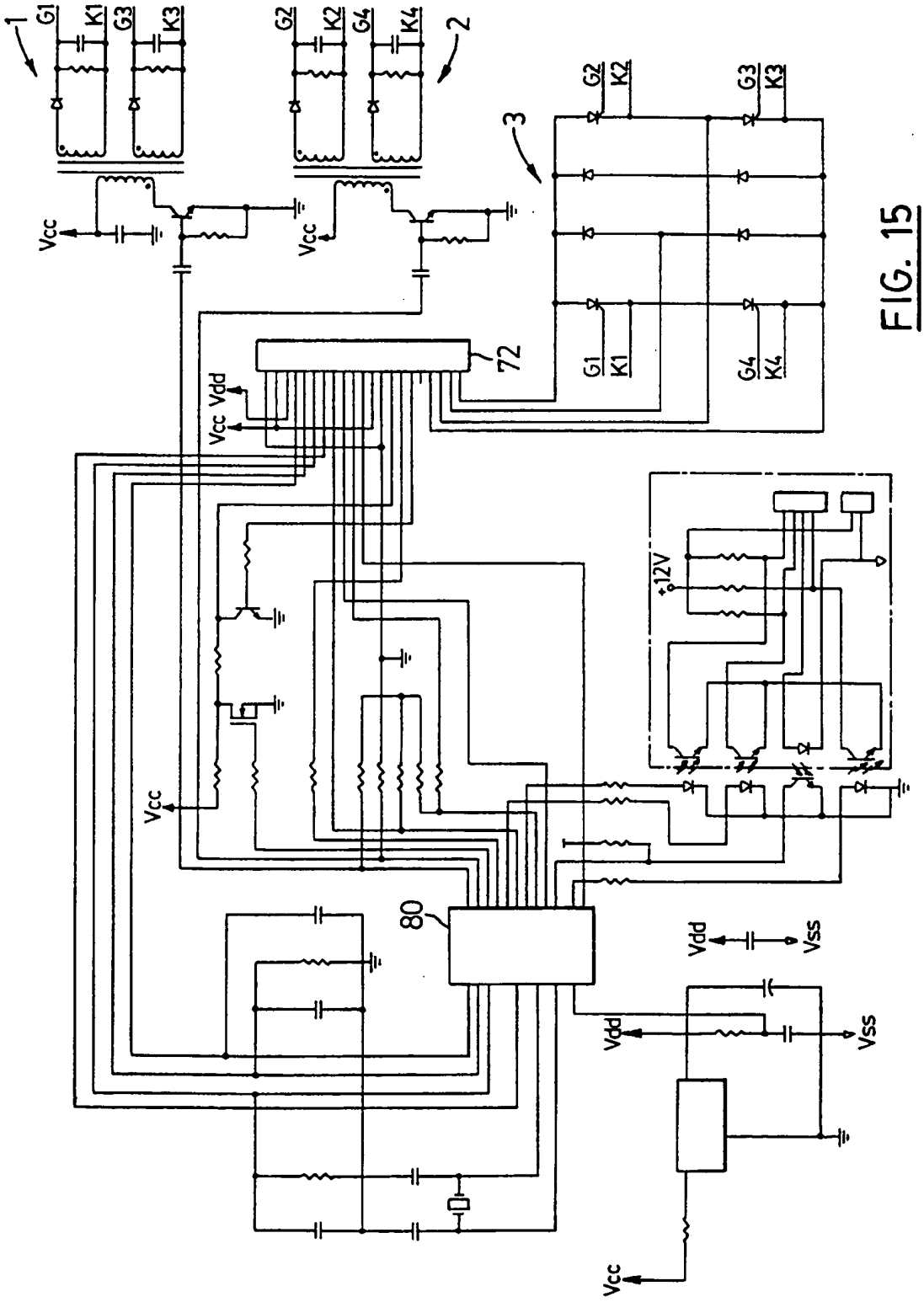

1
G1
K1
G3
K3
G2
K2
G4
K4
2
3
Vcc
Vcc
G2
K2
G3
K3
72
G1
K1
G4
K4
Vcc Vdd
+12V
Vcc
80
Vdd
Vss
Vdd
Vss
Vcc

FIG. 15

INTERNATIONAL SEARCH REPORT

International Application No
PCT/CA 98/00602

A. CLASSIFICATION OF SUBJECT MATTER

H 02 M 7/521,H 02 M 7/525,H 02 J 9/06,H 02 H 7/122

According to International Patent Classification (IPC) or to both national classification and IPC6

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H 02 M,H 02 J,H 02 H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4208711 A (BAKER, R.H.) 17 June 1980 (17.06.80), column 4, line 11 - column 5, line 23, fig. 1,4. --	1,16
A	US 4410935 A (DANG, G.S.) 18 October 1983 (18.10.83), column 3, lines 5-47. ----	1,5,7, 16

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
04 August 1998	08. 10. 98

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	MEHLMAUER e.h.

Form PCT/ISA/210 (second sheet) (July 1992)

ANHANG

zum internationalen Recherchenbericht über die internationale Patentanmeldung Nr.

ANNEX

to the International Search Report to the International Patent Application No.

ANNEXE

au rapport de recherche international relatif à la demande de brevet international n°

PCT/CA 98/00602 SAE 198236

In diesem Anhang sind die Mitglieder der Patentfamilien der im obengenannten internationalen Recherchenbericht angeführten Patentdokumente angegeben. Diese Angaben dienen nur zur Unterrichtung und erfolgen ohne Gewähr.

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The Office is in no way liable for these particulars which are given merely for the purpose of information.

La présénte annexe indique les membres de la famille de brevets relatifs aux documents de brevets cités dans le rapport de recherche international visée ci-dessus. Les renseignements fournis sont donnés à titre indicatif et n'engagent pas la responsibilité de l'Office.

Im Recherchenbericht angeführtes Patentdokument Patent document cited in search report Document de brevet cité dans le rapport de recherche	Datum der Veröffentlichung Publication date Date de publication	Mitglied(er) der Patentfamilie Patent family member(s) Membre(s) de la famille de brevets	Datum der Veröffentlichung Publication date Date de publication
US A 4208711	17-06-80	keine - none - rien	
US A 4410935	18-10-83	AU A1 81772/82	30-09-82
		AU B2 546821	19-09-85
		CA A1 1173499	28-08-84
		GB A1 2095486	29-09-82
		GB B2 2095486	17-10-84

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☐ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.